DATA SHEET

SUNPLUS

SPCA504B

Dual Mode PC Camera Processor

Preliminary

JUL. 16, 2003

Version 0.1

Table of Contents

PAGE

DUAL MODE PC CAMERA PROCESSOR

1.GENERAL DESCRIPTION

The SPCA504B is a digital camera processor chip that provides a complete solution for dual mode camera applications. This chip integrates image sensor interface, digital video input interface, color image processor, storage media controller, JPEG image compression engine, USB interface, and a built-in micro-controller to fulfill all dual-mode camera requirements. The SPCA504B supports both progressive CCD and CMOS image sensors up to 1.1M and 2.0M pixels respectively. The SPCA504B camera processor chip includes, not only the latest technology, but also the full services and support of Sunplus.

2.FEATURE

■ The main functions of the SPCA504B include:
- — DSC mode for capturing one frame at a time
- — Video clip mode for capturing video with a frame rate of 15~30 frames/sec
- — PC-camera mode at 30 frames/sec for CIF size, 20 frames/sec for VGA size

■ The SPCA504B chip has many image-processing functions that include:
- — High quality color interpolation
- — Two-dimensional edge enhancement
- — Bad pixels concealment
- — AE/AWB parameter windows cover a full range of sensors

■ The SPCA504B supports progressive image sensors up to 1.3M/2.1M pixels. Some of them are listed below:

CCD
- — VGA : Sharp LZ24BP, Sony ICX098AK, Panasonic MN3777
- — XGA : Sony ICX204AK
- — SXGA : Panasonic MN3778 (progressive)

CMOS
- — VGA: Agilent HDCS2020/21, Micron MI-330, OmniVision OV7620, Hynix HV7131D/E, Sharp LZ34B10, PixArt PAS202, TASC TAS5130A, Biomorphic BI8602, IC Media ICM205DL, Motorola SCM20014, National Semiconductor LM9627, Century Semiconductor CS2102, Toshiba TCM5043LU
- — SVGA: Hynix HV7141B
- — SXGA: Motorola MCM20027, OmniVision OV9620, IC Media ICM108T, TASC 5160, PixArt PAS005B, STMicroelectronics VV6600
- — UXGA: OmniVision OV2610, IC Media ICM109T,

■ Audio functions that the SPCA504B supports include audio class, audio capture, audio record and playback as provided by the following:
- — bi-directional AC-link interface for audio record and playback
- — MP3 decoder interface for MP3 decoding and playback
- — microphone interface for audio record
- — IMA-ADPCM compatible ADPCM compression engine for audio compression

■ In addition to the external SDRAM module, the SPCA504B supports a large variety of storage media including:
- — NAND-gate flash memory (smart media card)
- — NOR-type flash memory
- — ATAPI interface (ATAPI CDRW, compact flash memory)
- — SPI serial flash memory, both mode0 and mode 3 supported (MultiMediaCard)
- — Next Flash serial flash memory
- — SD Card

■ The DRAM interface supports 16M bits and 64M bits SDRAM modules through a 16-bit data bus.

■ The SPCA504B supports JPEG image compression in YUV422 and YUV 420 chroma formats. It can also compress BW (black-and-white) images. The output data format is compliant with the JFIF bit-stream format. An automatic scale-down function is included to fit into the display size in the playback mode.

■ The USB interface supports the following pipes to the PC:
- — Video ISO-IN pipe for video data transmission to the PC
- — Audio ISO-IN pipe for Audio data transmission to the PC
- — BULK-IN pipe for uploading images from the camera to the PC
- — BULK-OUT pipe for downloading image data, audio data, firmware, and MP3 data to the camera
- — INTERRUPT-IN pipe for reporting camera status and events to the PC
- — Hardware support for Mass Storage Device Class (MSDC)

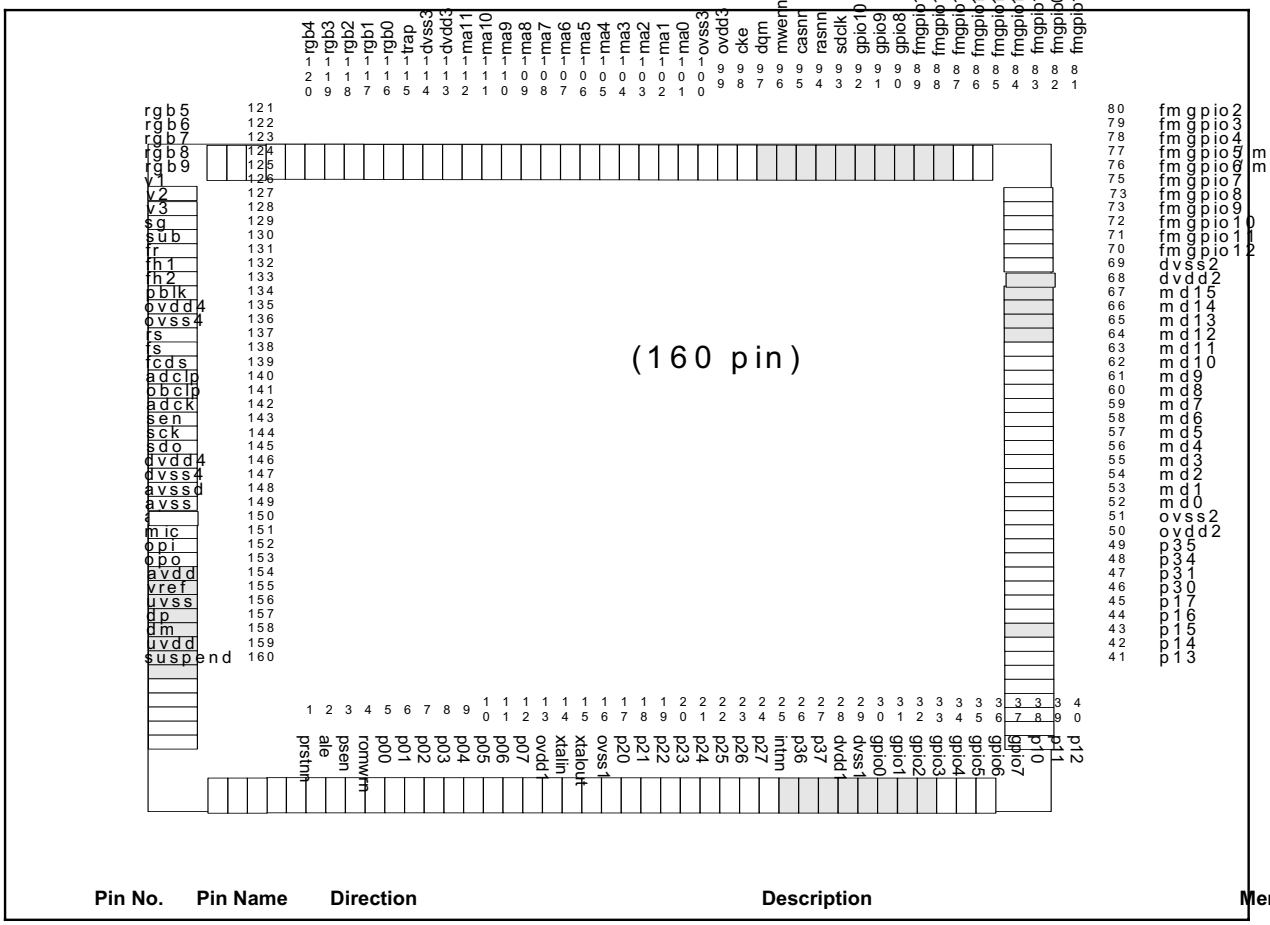
■ The SPCA504B has a built-in 8032 micro-controller with 6K bytes of internal SRAM

— Supports *ISP* (in-system-programming) with 4K bytes of shadow space
— Has built-in 64K bytes of mask ROM
— Supports *LOW-POWER* mode and *IDLE* mode

■ The SPCA504B also:
— Has a built-in PLL to supply on-chip clock sources
— Provides packaging in either 128-pin QFP or 160-pin LQFP
— Uses a 3.3/2.5 dual power supply

3.PIN DESCRIPTION

3.1. Pin Assignment For 160-Pin Package (P1 Package)



Pin No.	Pin Name	Direction	Description		Memo
			System Interface		
	1 PRSTNN	I	Power-on reset		
			CPU Interface		
2	ALE	B	Address latch enable This pin is an output pin when the built-in CPU is enabled. When an external CPU is used, this pin is an input pin.		
3	PSEN	B	Program space enable This pin is an output pin when the built-in CPU is enabled. When an external CPU is used, this pin is an input pin.		
4	ROMWRNN	O	External write pulse. This pin is used in the ISP (in-system-programming) function.	GPIO11	
5	P00	B	CPU port 0, address/data multiplex pin, bit 0.		
6	P01	B	CPU port 0, address/data multiplex pin, bit 1.		
7	P02	B	CPU port 0, address/data multiplex pin, bit 2.		
8	P03	B	CPU port 0, address/data multiplex pin, bit 3.		
9	P04	B	CPU port 0, address/data multiplex pin, bit 4.		
10	P05	B	CPU port 0, address/data multiplex pin, bit 5.		

Pin No.	Pin Name	Direction	Description			Memo
11	P06	B	CPU port 0, address/data multiplex pin, bit 6.			
12	P07	B	CPU port 0, address/data multiplex pin, bit 7.			
13	OVDD1	PG	IO power			3.3V
14	XTALIN	I	Crystal input			
15	XTALOUT	O	Crystal output			
16	OVSS1	PG	IO ground			
17	P20	B	CPU port 2, high byte address, bit 0. This bus is an output bus in the internal CPU mode. It is an input bus in the external CPU mode.			
18	P21	B	CPU port 2, high byte address, bit 1.			
19	P22	B	CPU port 2, high byte address, bit 2.			
20	P23	B	CPU port 2, high byte address, bit 3.			
21	P24	B	CPU port 2, high byte address, bit 4.			
22	P25	B	CPU port 2, high byte address, bit 5.			
23	P26	B	CPU port 2, high byte address, bit 6.			
24	P27	B	CPU port 2, high byte address, bit 7.			
25	INTnn	B	When the internal CPU is enabled, this pin is an input pin. External interrupt events can be passed to the built-in CPU via this pin. When using an external CPU, this pin is an output pin that is driven low by SPCA504B internal module interrupt events.			
26	P36	B	CPU port 3, bit 6.			WRnn
27	P37	B	CPU port 3, bit 7.			RDnn
28	DVDD1	PG	Core power			2.5V
29	DVSS1	PG	Core ground			
30	GPIO0	B	General purpose IO			
31	GPIO1	B	General purpose IO			
32	GPIO2	B	General purpose IO			
33	GPIO3	B	General purpose IO			
34	GPIO4	B	General purpose IO			
35	GPIO5	B	General purpose IO			
36	GPIO6	B	General purpose IO			
37	GPIO7	B	General purpose IO			
Multi-function pin			8051	MP3/UI	AC-link	
38	P10	B	CPU port 1, bit 0	MP3/UI	AC-link	Note 1,2
39	P11	B	CPU port 1, bit 1	MPtxfs (O)	AUrstnn (O)	Note 1,2
40	P12	B	CPU port 1, bit 2	MPrxfs (O)	AUsync (O)	Note 1,2
41	P13	B	CPU port 1, bit 3	MPsiclk (O)	AUdout (O)	Note 1,2
42	P14	B	CPU port 1, bit 4	MPd (B)	AUbclk (I)	Note 1,2
43	P15	B	CPU port 1, bit 5	MPfceb1 (I)	AUdin (I)	Note 1
44	P16	B	CPU port 1, bit 6	MPfceb2 (I)		Note 1
45	P17/WKUP1	B	CPU port 1, nit 7	MPrstnn (O)		Note 4
46	P30/WKUP2	B		Uiclk (I)		TXD, Note4
47	P31	B		Uidi (I)		RXD, Note4
48	P34	B		Uido (O)		T0, Note 5

Pin No.	Pin Name	Direction	Description							Memo
49	P35	B	CPU port 3, bit 5	AUDck (O)						T1
50	OVDD2	PG	IO power							3.3V
51	OVSS2	PG	IO ground							
Sdram Interface (I)										
			The DRAM data bus is multiplexed with the storage media bus. Depending on the type of package, the multiplexed pins are different.							
				128-pin package	160-pin package					
52	MD0	B	SDRAM data bit 0.	FMGPIO8	FMGPIO20					
53	MD1	B	SDRAM data bit 1.	FMGPIO9	FMGPIO21					
54	MD2	B	SDRAM data bit 2.	FMGPIO10	FMGPIO22					
55	MD3	B	SDRAM data bit 3.	FMGPIO11	FMGPIO23					
56	MD4	B	SDRAM data bit 4.	FMGPIO12	FMGPIO24					
57	MD5	B	SDRAM data bit 5.	FMGPIO13	FMGPIO25					
58	MD6	B	SDRAM data bit 6.	FMGPIO14	FMGPIO26					
59	MD7	B	SDRAM data bit 7.	FMGPIO15	FMGPIO27					
60	MD8	B	SDRAM data bit 8.	FMGPIO16	FMGPIO28					
61	MD9	B	SDRAM data bit 9.	FMGPIO17	FMGPIO29					
62	MD10	B	SDRAM data bit 10.	FMGPIO18						
63	MD11	B	SDRAM data bit 11.	FMGPIO19						
64	MD12	B	SDRAM data bit 12.							
65	MD13	B	SDRAM data bit 13.							
66	MD14	B	SDRAM data bit 14.							
67	MD15	B	SDRAM data bit 15.							
68	DVDD2	PG	Core power							2.5V
69	DVSS2	PG	Core ground							
Storage Media Interface										
			The SPCA504B supports NAND-gate flash memory, nor-type flash memory, ATA interface, SPI interface, SD memory card and the NextFlash serial interface for the storage media. These interfaces share the 'fmgpio" bus. The pin definitions depend on the type of the storage media selected. If some pins of the "fmgpio" bus are not used in a specific type of storage media, they can be used as GPIO's for the system control. In the 128-pin application, the fmgpio[19:8] is not bonded. The SDRAM data bus is shared with the storage media bus.								
			NAND-gate	SMC	MMC (SPI)	SD	CFA memory	CFA (IDE)	Next Flash	NOR-type Flash
70	FMGPIO12	B	D0 (B)	D0 (B)			A1 (O)	A1 (O)		A17 (O)
71	FMGPIO11	B	WE/ (O)	WE/ (O)		D3 (B)	A0 (O)	A0 (O)		A16 (O)
72	FMGPIO10	B	RE/ (O)	RE/ (O)		D2 (B)	OE/ (O)	RD/ (O)		A15 (O)
73	FMGPIO9	B	WP/ (O)	WP/ (O)		D1 (B)	WE/ (O)	WR/ (O)		A14 (O)
74	FMGPIO8	B	CLE (O)	CLE(O)	SO (O)	D0 (B)	RST/ (O)	RST/ (O)		A13 (O)
75	FMGPIO7	B			SI (I)		RDY/ (I)	IRQ (I)		A12 (O)
76	FMGPIO6 /MA13	B		RDY (I)	WP/ (O)		WAIT/ (I)	IORDY (I)		A11 (O)
77	FMGPIO5 /MA12	B		CD1 (I)	RST/ (O)		CD1 (I)	CD1 (I)		A10 (O)

Pin No.	Pin Name	Direction	Description							Memo
78	FMGPIO4	B	ALE (O)	ALE (O)	SCK (O)		CD2 (I)	CD2 (I)		A9 (O)
79	FMGPIO3	B			RDY (I)	CLK (O)	REG/ (O)	CS2/ (O)		A8 (O)
80	FMGPIO2	B		CE/ (O)	CS/ (O)	CMD (B)	CE/ (O)	CS1/ (O)		RST/ (O)
81	FMGPIO1	B	RDY (I)						SIO (B)	RDY (I)
82	FMGPIO0	B	CE/ (O)						SCK (O)	CE/ (O)
83	FMGPIO13	B	D1 (B)	D1 (B)			A2 (O)	A2 (O)		A18 (O)
84	FMGPIO14	B	D2 (B)	D2 (B)			D0 (B)	D0 (B)		A19 (O)
85	FMGPIO15	B	D3 (B)	D3 (B)			D1 (B)	D1 (B)		A20 (O)
86	FMGPIO16	B	D4 (B)	D4 (B)			D2 (B)	D2 (B)		A21 (O)
87	FMGPIO17	B	D5 (B)	D5 (B)			D3 (B)	D3 (B)		
88	FMGPIO18	B	D6 (B)	D6 (B)			D4 (B)	D4 (B)		
89	FMGPIO19	B	D7 (B)	D7 (B)			D5 (B)	D5 (B)		
90	GPIO8	B							A16	Note 7
91	GPIO9	B							A17	Note 7
92	GPIO10	B							SG2	Note 7
SDRAM Interface (II)										
93	SDCLK	O	SDRAM clock						GPIO12	
94	RASnn	O	SDRAM raw address strobe signal							
95	CASnn	O	SDRAM column address strobe signal							
96	MWEnn	O	SDRAM write enable signal							
97	DQM	O	SDRAM data mask signal							
98	CKE	O	SDRAM clock enable signal						GPIO13	
99	OVDD3	PG	IO power							3.3V
100	OVSS3	PG	IO ground							
101	MA0	B	SDRAM address bit 0. This bus is also used as the IO-trap. During the IO-trap stage, the “MA” bus is an input bus. After the IO-trap stage, the “MA” bus is an output bus.							
102	MA1	B	SDRAM address bit 1							
103	MA2	B	SDRAM address bit 2							
104	MA3	B	SDRAM address bit 3							
105	MA4	B	SDRAM address bit 4							
106	MA5	B	SDRAM address bit 5							
107	MA6	B	SDRAM address bit 6							
108	MA7	B	SDRAM address bit 7							
109	MA8	B	SDRAM address bit 8							
110	MA9	B	SDRAM address bit 9							
111	MA10	B	SDRAM address bit 10							
112	MA11	B	SDRAM address bit 11							
113	DVDD3	PG	Core power							2.5V
114	DVSS3	PG	Core ground							

Pin No.	Pin Name	Direction	Description			Memo
115	TRAP	B	IO-trap control signal. The configuration of the SPCA504B is partly controlled by the IO-trap values in the SDRAM address bus. This trap signal controls the power of the pull-up resistors attached to the SDRAM address. The signal is high once the SPCA504B power is applied, and will go low after the chip reset is completed. This signal will remain low during SPCA504B operation and in the suspend state. This pin may be configured as a GPIO pin after power-on.		GPIO14	
116	RGB0	I	Sensor data input bit 0. (internal pull low)			
117	RGB1	I	Sensor data input bit 1. (internal pull low)			
118	RGB2	I	Sensor data input bit 2. (internal pull low)			
119	RGB3	I	Sensor data input bit 3. (internal pull low)			
120	RGB4	I	Sensor data input bit 4. (internal pull low)			
121	RGB5	I	Sensor data input bit 5. (internal pull low)			
122	RGB6	I	Sensor data input bit 6. (internal pull low)			
123	RGB7	I	Sensor data input bit 7. (internal pull low)			
124	RGB8	I	Sensor data input bit 8. (internal pull low)			
125	RGB9	I	Sensor data input bit 9. (internal pull low)			
Timing Generator						
			Default function	TG disabled		
126	V1	B	Clock output for vertical CCD drive	EXTvd (B)		Note 6
127	V2	B	Clock output for vertical CCD drive	EXThd (B)		Note 6
128	V3	B	Clock output for vertical CCD drive	EXTvvalid (I)	GPIO15	Note 6
129	SG	B	CCD readout pulse	EXThvalid (I)	GPIO16	Note 6
130	SUB	O	CCD electric charge sweep pulse output.	EXTdvalid (I)	GPIO17	Note 6
131	FR	O	CCD reset gate pulse	EXTfield (I)	GPIO18	Note 6
132	FH1	O	Clock output for horizontal CCD drive		GPIO19	
133	FH2	O	Clock output for horizontal CCD drive		GPIO20	
134	PBLK	O	CCD blanking cleaning pulse.		GPIO21	
135	OVDD4	PG	Timing generator IO PAD power			3.3V
136	OVSS4	PG	Timing generator IO PAD ground			
137	RS	O	Sample and hold pulse.		GPIO22	
138	FS	O	CDS control signal.		GPIO23	
139	FCDS	O	CDS control signal		GPIO24	
140	ADCLP	B	Dummy pixel clamping signal	2XCK output		Note 6
141	OBCLP	O	Optical black clamping signal		GPIO25	
142	ADCK	B	Clock output for AD converter.	1XCK output		Note 6
143	SEN	O	Serial interface data transaction starting signal. The SPCA504B has a built-in synchronous serial interface to communicate with the CDS/AGC chip. The CDS/AGC chip is needed when the SPCA504B is connected with a CCD image sensor.		GPIO26	
144	SCK	O	CDS/AGC serial interface clock.	SSISCL		Note 6
145	SD	B	CDS/AGC interface data output.	SSISDA		Note 6
146	DVDD4	PG	Core power	2.5V		
147	DVSS4	PG	Core ground			

Pin No.	Pin Name	Direction	Description		Memo
			Built-in Audio ADC		
148	AVSSD	PG	ADC ground (digital)		
149	AVSS	PG	ADC ground (analog)		
150	ALC	I	AGC gain control		
151	MIC	I	Microphone analog input		
152	OPI	I	AGC OpAmp input		
153	OPO	O	AGC OpAmap output		
154	AVDD	PG	ADC power (analog)		3.3V
155	VREF	O	ADC voltage reference		
			USB Transceiver		
156	UVSS	PG	USB transceiver ground		
157	DP	B	USB D+ signal		
158	DM	B	USB D- signal		
159	UVDD	PG	USB transceiver power		3.3V
160	SUSPEND	O	Chip suspend output	GPIO27	

Note 1. MP3 interface

Pin 38 to 44 can be programmed as an MP3 data interface. The pin sequence is defined in the following table:

Pin	Name	Direction	Description
38	MPtxfs	O	Data transmit frame sync.
39	MPrxfs	O	Data receiving frame sync.
40	Mpsiclk	O	Serial interface serial clock
41	MPd	B	Serial data bit
42	Mpfceb1	I	MP3 decoder status 1
43	Mpfceb2	I	MP3 decoder status 2
44	MPrstnn	O	MP3 decoder reset signal

Note 2. AC-link

Pin 38 to pin 42 can be programmed as an AC-link interface. The pin sequence is defined in the following table. Note that theAC-97 interface pins are shared with the MP3 interface. MP3 and AC-97 functions shall not exist at the same time in normal applications.

Pin	Name	Direction	Description
38	AUrstnn	O	AC-link reset signal
39	AUsync	O	AC-link synchronization signal
40	AUdout	O	AC-link data output pin
41	AUbclk	I	AC-link audio bit clock
42	AUdin	I	AC-link data input pin

Note 3. Pin 45 to 47 can be used as the UI module interface. The pin definition is in the following table:

Pin	Name	Direction	Description
45	Uiclk	I	UI clock
46	Uidi	I	UI data input (from UI module to SPCA504B)
47	Uido	O	UI data output(from SPCA504B to UI module)

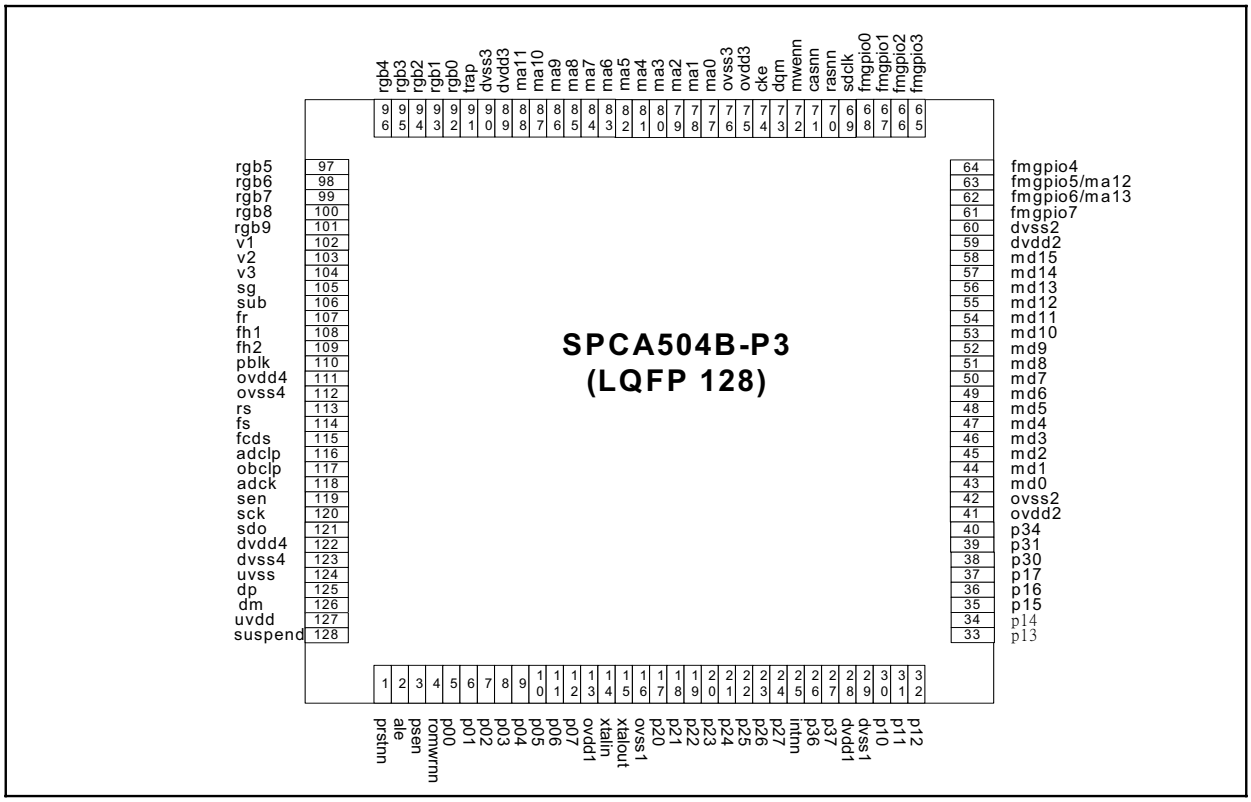
Note 4. Pin 48 can be used to output a clock for external audio devices, such as MP3 decoder or AC-97 CODEC. The frequency of the audio clock can be 12MHz, 19MHz or 24 MHz.

Note 5. The TG (timing generator) interface is designed for CCD timing generation. If the application uses a TV decoder or a CMOS sensor as the image input device, the TG output pins can be programmed to their alternative functions. In the CMOS application, the sync signals and clocks can be provided by the CMOS sensor or by the SPCA504B. To use the clock provided by an external device, the application must turn off the corresponding output enable registers. The synchronous serial interface is used to program the registers of the TV decoders and CMOS sensors.

Pin	Name	Direction	Description
126	Extvd	B	External vertical sync. Signal
127	Exthd	B	External horizontal sync. Signal
128	Extvvalid	I	External vertical valid, for TV decoder
129	Exthvalid	I	External horizontal valid, for TV decoder
130	Extdvalid	I	External data valid, for TV decoder
131	Extfield	I	External field signal, for TV decoder
140	2XCK	B	Pixel clock X2
142	1XCK	B	Pixel clock X1
144	SSISCL	O	Synchronous serial interface clock
145	SSISDA	B	Synchronous serial interface data

Note 6. Pin A16 and A17 are ROM address pins. They are used to extend the ROM space to 256KB. SG is a signal for the CCD TG interface.

3.2. Pin Assignment For 128-Pin Package (P3 Package)



Pin No.	Pin Name	Direction	Description			Memo
System Interface						
1	PRSTNN	I	Power-on reset			
CPU Interface						
2	ALE	B	Address latch enable This pin is an output pin when the built-in CPU is enabled. When an external CPU is used, this pin is an input pin.			
3	PSEN	B	Program space enable This pin is an output pin when the built-in CPU is enabled. When external CPU is used, this pin is an input pin.			
4	ROMWRNN	O	External write pulse. This pin is used in the ISP (in-system-programming) function.	GPIO11		
5	P00	B	CPU port 0, address/data multiplex pin, bit 0.			
6	P01	B	CPU port 0, address/data multiplex pin, bit 1.			
7	P02	B	CPU port 0, address/data multiplex pin, bit 2.			
8	P03	B	CPU port 0, address/data multiplex pin, bit 3.			
9	P04	B	CPU port 0, address/data multiplex pin, bit 4.			
10	P05	B	CPU port 0, address/data multiplex pin, bit 5.			
11	P06	B	CPU port 0, address/data multiplex pin, bit 6.			
12	P07	B	CPU port 0, address/data multiplex pin, bit 7.			
13	OVDD1	PG	IO power			3.3V
14	XTALIN	I	Crystal input			
15	XTALOUT	O	Crystal output			
16	OVSS1	PG	IO ground			
17	P20	B	CPU port 2, high byte address, bit 0. This bus is an output bus in the internal CPU mode. It is an input bus in the external CPU mode.			
18	P21	B	CPU port 2, high byte address, bit 1.			
19	P22	B	CPU port 2, high byte address, bit 2.			
20	P23	B	CPU port 2, high byte address, bit 3.			
21	P24	B	CPU port 2, high byte address, bit 4.			
22	P25	B	CPU port 2, high byte address, bit 5.			
23	P26	B	CPU port 2, high byte address, bit 6.			
24	P27	B	CPU port 2, high byte address, bit 7.			
25	INTnn	B	When the internal CPU is enabled, this pin is an input pin. External interrupt events can be passed to the built-in CPU via this pin. When using external CPU, this pin is an output pin that is driven low by SPCA504B internal module interrupt events.			
26	P36	B	CPU port 3, bit 6.			WRnn
27	P37	B	CPU port 3, bit 7.			RDnn
28	DVDD1	PG	Core power			2.5V
29	DVSS1	PG	Core ground			
Multi-Function Pin			8051	MP3/UI	AC-link	
30	P10	B	CPU port 1, bit 0	MPtxfs (O)	AUrstnn (O)	Note 1,2
31	P11	B	CPU port 1, bit 1	MPrxfs (O)	AUsync (O)	Note 1,2

Pin No.	Pin Name	Direction	Description			Memo
32	P12	B	CPU port 1, bit 2	MPsiclk (O)	AUdout (O)	Note 1,2
33	P13	B	CPU port 1, bit 3	MPd (B)	AUbclk (I)	Note 1,2
34	P14	B	CPU port 1, bit 4	MPfceb1 (I)	AUdin (I)	Note 1,2
35	P15	B	CPU port 1, bit 5	MPfceb2 (I)		Note 1
36	P16	B	CPU port 1, bit 6	MPrstnn (O)		Note 1
37	P17/WKUP1	B	CPU port 1, nit 7	Uiclk (I)		Note 4
38	P30/WKUP2	B		Uidi (I)		TXD, Note4
39	P31	B		Uido (O)		RXD, Note4
40	P34	B		AUDck (O)		T0, Note 5
41	OVDD2	PG	IO power			3.3V
42	OVSS2	PG	IO ground			
SDRAM Interface (I)						
			The DRAM data bus is multiplexed with the storage media bus. Depending on the type of the package, the multiplexed pins are different.			
				128-pin package	160-pin package	
43	MD0	B	SDRAM data bit 0.	FMGPIO8	FMGPIO20	
44	MD1	B	SDRAM data bit 1.	FMGPIO9	FMGPIO21	
45	MD2	B	SDRAM data bit 2.	FMGPIO10	FMGPIO22	
46	MD3	B	SDRAM data bit 3.	FMGPIO11	FMGPIO23	
47	MD4	B	SDRAM data bit 4.	FMGPIO12	FMGPIO24	
48	MD5	B	SDRAM data bit 5.	FMGPIO13	FMGPIO25	
49	MD6	B	SDRAM data bit 6.	FMGPIO14	FMGPIO26	
50	MD7	B	SDRAM data bit 7.	FMGPIO15	FMGPIO27	
51	MD8	B	SDRAM data bit 8.	FMGPIO16	FMGPIO28	
52	MD9	B	SDRAM data bit 9.	FMGPIO17	FMGPIO29	
53	MD10	B	SDRAM data bit 10.	FMGPIO18		
54	MD11	B	SDRAM data bit 11.	FMGPIO19		
55	MD12	B	SDRAM data bit 12.			
56	MD13	B	SDRAM data bit 13.			
57	MD14	B	SDRAM data bit 14.			
58	MD15	B	SDRAM data bit 15.			
59	DVDD2	PG	Core power			2.5V
60	DVSS2	PG	Core ground			
Storage Media Interface						
			The SPCA504B supports NAND-gate flash memory, nor-type flash memory, ATA interface, SPI interface, SD memory card and the NextFlash serial interface for storage media. These interfaces share the ‘fmgpio“ bus. The pin definitions depend on the type of storage media selected. If some pins of the “fmgpio” bus are not used in a specific type of the storage media, they can be used as GPIO’s for the system control. In the 128-pin application the fmgpio[19:8] is not bonded. The SDRAM data bus is shared with the storage media bus.			

Pin No.	Pin Name	Direction	Description							Memo
			NAND-gate	SMC	MMC (SPI)	SD	CFA memory	CFA (IDE)	Next Flash	NOR-type Flash
*47	FMGPIO12	B	D0 (B)	D0 (B)			A1 (O)	A1 (O)		A17 (O)
*46	FMGPIO11	B	WE/ (O)	WE/ (O)		D3 (B)	A0 (O)	A0 (O)		A16 (O)
*45	FMGPIO10	B	RE/ (O)	RE/ (O)		D2 (B)	OE/ (O)	RD/ (O)		A15 (O)
*44	FMGPIO9	B	WP/ (O)	WP/ (O)		D1 (B)	WE/ (O)	WR/ (O)		A14 (O)
*43	FMGPIO8	B	CLE (O)	CLE(O)	SO (O)	D0 (B)	RST/ (O)	RST/ (O)		A13 (O)
61	FMGPIO7	B			SI (I)		RDY/ (I)	IRQ (I)		A12 (O)
62	FMGPIO6 /MA13	B		RDY (I)	WP/ (O)		WAIT/ (I)	IORDY (I)		A11 (O)
63	FMGPIO5 /MA12	B		CD1 (I)	RST/ (O)		CD1 (I)	CD1 (I)		A10 (O)
64	FMGPIO4	B	ALE (O)	ALE (O)	SCK (O)		CD2 (I)	CD2 (I)		A9 (O)
65	FMGPIO3	B			RDY (I)	CLK (O)	REG/ (O)	CS2/ (O)		A8 (O)
66	FMGPIO2	B		CE/ (O)	CS/ (O)	CMD (B)	CE/ (O)	CS1/ (O)		RST/ (O)
67	FMGPIO1	B	RDY (I)						SIO (B)	RDY (I)
68	FMGPIO0	B	CE/ (O)						SCK (O)	CE/ (O)
*48	FMGPIO13	B	D1 (B)	D1 (B)			A2 (O)	A2 (O)		A18 (O)
*49	FMGPIO14	B	D2 (B)	D2 (B)			D0 (B)	D0 (B)		A19 (O)
*50	FMGPIO15	B	D3 (B)	D3 (B)			D1 (B)	D1 (B)		A20 (O)
*51	FMGPIO16	B	D4 (B)	D4 (B)			D2 (B)	D2 (B)		A21 (O)
*52	FMGPIO17	B	D5 (B)	D5 (B)			D3 (B)	D3 (B)		
*53	FMGPIO18	B	D6 (B)	D6 (B)			D4 (B)	D4 (B)		
*54	FMGPIO19	B	D7 (B)	D7 (B)			D5 (B)	D5 (B)		
SDRAM Interface (II)										
69	SDCLK	O	SDRAM clock						GPIO12	
70	RASnn	O	SDRAM raw address strobe signal							
71	CASnn	O	SDRAM column address strobe signal							
72	MWEnn	O	SDRAM write enable signal							
73	DQM	O	SDRAM data mask signal							
74	CKE	O	SDRAM clock enable signal						GPIO13	
75	OVDD3	PG	IO power							3.3V
76	OVSS3	PG	IO ground							
77	MA0	B	SDRAM address bit 0 This bus is also used as the IO-trap. During the IO-trap stage, the “MA” bus is an input bus. After the IO-trap stage, this bus is an output bus.							
78	MA1	B	SDRAM address bit 1							
79	MA2	B	SDRAM address bit 2							
80	MA3	B	SDRAM address bit 3							
81	MA4	B	SDRAM address bit 4							
82	MA5	B	SDRAM address bit 5							
83	MA6	B	SDRAM address bit 6							
84	MA7	B	SDRAM address bit 7							
85	MA8	B	SDRAM address bit 8							

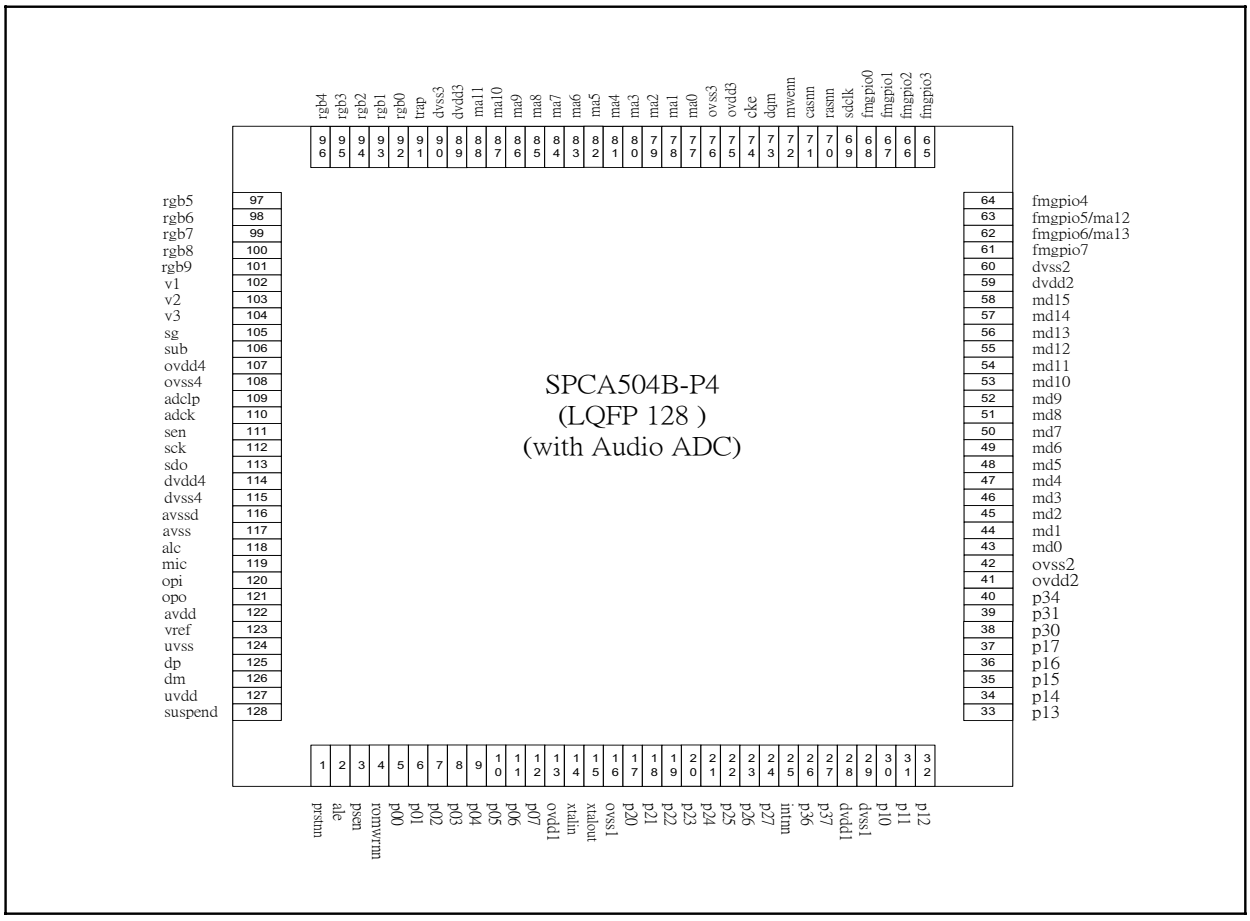
Pin No.	Pin Name	Direction	Description			Memo
86	MA9	B	SDRAM address bit 9			
87	MA10	B	SDRAM address bit 10			
88	MA11	B	SDRAM address bit 11			
89	DVDD3	PG	Core power			2.5V
90	DVSS3	PG	Core ground			
91	TRAP	B	IO-trap control signal The configuration of the SPCA504B is partly controlled by the IO-trap values in the SDRAM address bus. This trap signal controls the power of the pull-up resistors attached to the SDRAM address. The signal is high once the SPCA504B power is applied and will go to low after the chip reset is completed. This signal will remain low during the SPCA504B operation and suspend states. This pin may be configured to be a GPIO pin after power-on.		GPIO14	
92	RGB0	I	Sensor data input bit 0. (internal pull low)			
93	RGB1	I	Sensor data input bit 1. (internal pull low)			
94	RGB2	I	Sensor data input bit 2. (internal pull low)			
95	RGB3	I	Sensor data input bit 3. (internal pull low)			
96	RGB4	I	Sensor data input bit 4. (internal pull low)			
97	RGB5	I	Sensor data input bit 5. (internal pull low)			
98	RGB6	I	Sensor data input bit 6. (internal pull low)			
99	RGB7	I	Sensor data input bit 7. (internal pull low)			
100	RGB8	I	Sensor data input bit 8. (internal pull low)			
101	RGB9	I	Sensor data input bit 9. (internal pull low)			
Timing Generator						
			Default function	TG disabled		
102	V1	B	Clock output for vertical CCD drive	EXTvd (B)		Note 6
103	V2	B	Clock output for vertical CCD drive	EXThd (B)		Note 6
104	V3	B	Clock output for vertical CCD drive	EXTvvalid (I)	GPIO15	Note 6
105	SG	B	CCD readout pulse	EXThvalid (I)	GPIO16	Note 6
106	SUB	O	CCD electric charge sweep pulse output.	EXTdvalid (I)	GPIO17	Note 6
107	FR	O	CCD reset gate pulse	EXTfield (I)	GPIO18	Note 6
108	FH1	O	Clock output for horizontal CCD drive		GPIO19	
109	FH2	O	Clock output for horizontal CCD drive		GPIO20	
110	PBLK	O	CCD blanking cleaning pulse.		GPIO21	
111	OVDD4	PG	Timing generator IO PAD power			3.3V
112	OVSS4	PG	Timing generator IO PAD ground			
113	RS	O	Sample and hold pulse.		GPIO22	
114	FS	O	CDS control signal.		GPIO23	
115	FCDS	O	CDS control signal		GPIO24	
116	ADCLP	B	Dummy pixel clamping signal	2XCK output		Note 6
117	OBCLP	O	Optical black clamping signal		GPIO25	
118	ADCK	B	Clock output for AD converter.	1XCK output		Note 6

Pin No.	Pin Name	Direction	Description			Memo
119	SEN	O	Serial interface data transaction starting signal. The SPCA504B has a built-in synchronous serial interface to communicate with the CDS/AGC chip. The CDS/AGC chip is needed when the SPCA504B is connected with a CCD image sensor.		GPIO26	
120	SCK	O	CDS/AGC serial interface clock.	SSISCL		Note 6
121	SDO	B	CDS/AGC interface data output.	SSISDA		Note 6
122	DVDD4	PG	Core power			2.5V
123	DVSS4	PG	Core ground			
USB Transceiver						
124	UVSS	PG	USB transceiver ground			
125	DP	B	USB D+ signal			
126	DM	B	USB D- signal			
127	UVDD	PG	USB transceiver power			3.3V
128	SUSPEND	O	Chip suspend output		GPIO27	

Note: When the 128-pin package is selected, FMGPIO8 to FMGPIO19 are multiplexed to MD0 to MD11.

Note 1-6 Please refer to Note 1-6 in Section 3.1 for the function descriptions while ignoring the pin numbers.

3.3. Pin assignment for 128-pin package with Audio ADC (P4 Package)



Pin No.	Pin Name	Direction	Description	Memo
			System Interface	
1	PRSTNN	I	Power-on reset	
			CPU Interface	
2	ALE	B	Address latch enable This pin is an output pin when the built-in CPU is enabled. When an external CPU is used, this pin is an input pin.	
3	PSEN	B	Program space enable This pin is an output pin when the built-in CPU is enabled. When an external CPU is used, this pin is an input pin.	
4	ROMWRNN	O	External write pulse This pin is used in the ISP (in-system-programming) function. GPIO11	
5	P00	B	CPU port 0, address/data multiplex pin, bit 0.	
6	P01	B	CPU port 0, address/data multiplex pin, bit 1.	
7	P02	B	CPU port 0, address/data multiplex pin, bit 2.	
8	P03	B	CPU port 0, address/data multiplex pin, bit 3.	
9	P04	B	CPU port 0, address/data multiplex pin, bit 4.	
10	P05	B	CPU port 0, address/data multiplex pin, bit 5.	
11	P06	B	CPU port 0, address/data multiplex pin, bit 6.	

Pin No.	Pin Name	Direction	Description			Memo
12	P07	B	CPU port 0, address/data multiplex pin, bit 7.			
13	OVDD1	PG	IO power			3.3V
14	XTALIN	I	Crystal input			
15	XTALOUT	O	Crystal output			
16	OVSS1	PG	IO ground			
17	P20	B	CPU port 2, high byte address, bit 0. This bus is an output bus in the internal CPU mode. It is an input bus in the external CPU mode.			
18	P21	B	CPU port 2, high byte address, bit 1.			
19	P22	B	CPU port 2, high byte address, bit 2.			
20	P23	B	CPU port 2, high byte address, bit 3.			
21	P24	B	CPU port 2, high byte address, bit 4.			
22	P25	B	CPU port 2, high byte address, bit 5.			
23	P26	B	CPU port 2, high byte address, bit 6.			
24	P27	B	CPU port 2, high byte address, bit 7.			
25	INTnn	B	When the internal CPU is enabled, this pin is an input pin. External interrupt events can be passed to the built-in CPU via this pin. When using an external CPU, this pin is an output pin that is driven low by SPCA504B internal module interrupt events.			
26	P36	B	CPU port 3, bit 6.			WRnn
27	P37	B	CPU port 3, bit 7.			RDnn
28	DVDD1	PG	Core power			2.5V
29	DVSS1	PG	Core ground			
Multi-Function Pin			8051	MP3/UI	AC-link	
30	P10	B	CPU port 1, bit 0	MPtxfs (O)	AUrstnn (O)	Note 1,2
31	P11	B	CPU port 1, bit 1	MPrxfs (O)	AUsync (O)	Note 1,2
32	P12	B	CPU port 1, bit 2	MPsiclk (O)	AUdout (O)	Note 1,2
33	P13	B	CPU port 1, bit 3	MPd (B)	AUbclk (I)	Note 1,2
34	P14	B	CPU port 1, bit 4	MPfceb1 (I)	AUdin (I)	Note 1,2
35	P15	B	CPU port 1, bit 5	MPfceb2 (I)		Note 1
36	P16	B	CPU port 1, bit 6	MPrstnn (O)		Note 1
37	P17/WKUP1	B	CPU port 1, nit 7	Uiclk (I)		Note 4
38	P30/WKUP2	B		Uidi (I)		TXD, Note4
39	P31	B		Uido (O)		RXD, Note4
40	P34	B		AUDck (O)		T0, Note 5
41	OVDD2	PG	IO power			3.3V
42	OVSS2	PG	IO ground			
SDRAM Interface (I)						
			The DRAM data bus is multiplexed with the storage media bus. Depending on the type of package, the multiplexed pins are different.			
				128-pin package	160-pin package	
43	MD0	B	SDRAM data bit 0.	FMGPIO8	FMGPIO20	
44	MD1	B	SDRAM data bit 1.	FMGPIO9	FMGPIO21	
45	MD2	B	SDRAM data bit 2.	FMGPIO10	FMGPIO22	
46	MD3	B	SDRAM data bit 3.	FMGPIO11	FMGPIO23	

Pin No.	Pin Name	Direction	Description							Memo
47	MD4	B	SDRAM data bit 4.	FMGPIO12		FMGPIO24				
48	MD5	B	SDRAM data bit 5.	FMGPIO13		FMGPIO25				
49	MD6	B	SDRAM data bit 6.	FMGPIO14		FMGPIO26				
50	MD7	B	SDRAM data bit 7.	FMGPIO15		FMGPIO27				
51	MD8	B	SDRAM data bit 8.	FMGPIO16		FMGPIO28				
52	MD9	B	SDRAM data bit 9.	FMGPIO17		FMGPIO29				
53	MD10	B	SDRAM data bit 10.	FMGPIO18						
54	MD11	B	SDRAM data bit 11.	FMGPIO19						
55	MD12	B	SDRAM data bit 12.							
56	MD13	B	SDRAM data bit 13.							
57	MD14	B	SDRAM data bit 14.							
58	MD15	B	SDRAM data bit 15.							
59	DVDD2	PG	Core power							2.5V
60	DVSS2	PG	Core ground							
Storage Media Interface										
			The SPCA504B supports NAND-gate flash memory, nor-type flash memory, ATA interface, SPI interface, SD memory card and the NextFlash serial interface for storage media. These interfaces share the ‘fmgpio“ bus. The pin definitions depend on the type of storage media selected. If some pins of the “fmgpio” bus are not used in a specific type of storage media, they can be used as GPIO for the system control. In the 128-pin application the fmgpio[19:8] is not bonded. The SDRAM data bus is shared with the storage media bus.								
			NAND-gate	SMC	MMC (SPI)	SD	CFA memory	CFA (IDE)	Next Flash	NOR-type Flash
*47	FMGPIO12	B	D0 (B)	D0 (B)			A1 (O)	A1 (O)		A17 (O)
*46	FMGPIO11	B	WE/ (O)	WE/ (O)		D3 (B)	A0 (O)	A0 (O)		A16 (O)
*45	FMGPIO10	B	RE/ (O)	RE/ (O)		D2 (B)	OE/ (O)	RD/ (O)		A15 (O)
*44	FMGPIO9	B	WP/ (O)	WP/ (O)		D1 (B)	WE/ (O)	WR/ (O)		A14 (O)
*43	FMGPIO8	B	CLE (O)	CLE(O)	SO (O)	D0 (B)	RST/ (O)	RST/ (O)		A13 (O)
61	FMGPIO7	B			SI (I)		RDY/ (I)	IRQ (I)		A12 (O)
62	FMGPIO6 /MA13	B		RDY (I)	WP/ (O)		WAIT/ (I)	IORDY (I)		A11 (O)
63	FMGPIO5 /MA12	B		CD1 (I)	RST/ (O)		CD1 (I)	CD1 (I)		A10 (O)
64	FMGPIO4	B	ALE (O)	ALE (O)	SCK (O)		CD2 (I)	CD2 (I)		A9 (O)
65	FMGPIO3	B			RDY (I)	CLK (O)	REG/ (O)	CS2/ (O)		A8 (O)
66	FMGPIO2	B		CE/ (O)	CS/ (O)	CMD (B)	CE/ (O)	CS1/ (O)		RST/ (O)
67	FMGPIO1	B	RDY (I)						SIO (B)	RDY (I)
68	FMGPIO0	B	CE/ (O)						SCK (O)	CE/ (O)
*48	FMGPIO13	B	D1 (B)	D1 (B)			A2 (O)	A2 (O)		A18 (O)
*49	FMGPIO14	B	D2 (B)	D2 (B)			D0 (B)	D0 (B)		A19 (O)
*50	FMGPIO15	B	D3 (B)	D3 (B)			D1 (B)	D1 (B)		A20 (O)
*51	FMGPIO16	B	D4 (B)	D4 (B)			D2 (B)	D2 (B)		A21 (O)
*52	FMGPIO17	B	D5 (B)	D5 (B)			D3 (B)	D3 (B)		

Pin No.	Pin Name	Direction	Description	Memo
*53	FMGPIO18	B	D6 (B) / D6 (B) / / / D4 (B) / D4 (B) /	
*54	FMGPIO19	B	D7 (B) / D7 (B) / / / D5 (B) / D5 (B) /	
			SDRAM interface (II)	
69	SDCLK	O	SDRAM clock / GPIO12	
70	RASnn	O	SDRAM raw address strobe signal	
71	CASnn	O	SDRAM column address strobe signal	
72	MWEnn	O	SDRAM write enable signal	
73	DQM	O	SDRAM data mask signal	
74	CKE	O	SDRAM clock enable signal / GPIO13	
75	OVDD3	PG	IO power	3.3V
76	OVSS3	PG	IO ground	
77	MA0	B	SDRAM address bit 0 This bus is also used as the IO-trap. During the IO-trap stage, the “MA” bus is an input bus. After the IO-trap stage, this bus is an output bus.	
78	MA1	B	SDRAM address bit 1	
79	MA2	B	SDRAM address bit 2	
80	MA3	B	SDRAM address bit 3	
81	MA4	B	SDRAM address bit 4	
82	MA5	B	SDRAM address bit 5	
83	MA6	B	SDRAM address bit 6	
84	MA7	B	SDRAM address bit 7	
85	MA8	B	SDRAM address bit 8	
86	MA9	B	SDRAM address bit 9	
87	MA10	B	SDRAM address bit 10	
88	MA11	B	SDRAM address bit 11	
89	DVDD3	PG	Core power	2.5V
90	DVSS3	PG	Core ground	
91	TRAP	B	IO-trap control signal / GPIO14 The configuration of the SPCA504B is partly controlled by the IO-trap values in the SDRAM address bus. This trap signal controls the power of the pull-up resistors attached to the SDRAM address. The signal is high once the SPCA504B power is applied and will go to low after the chip reset is completed. This signal will remain low during SPCA504B operation and in the suspend state. This pin may be configured as a GPIO pin after power-on.	
92	RGB0	I	Sensor data input bit 0. (internal pull low)	
93	RGB1	I	Sensor data input bit 1. (internal pull low)	
94	RGB2	I	Sensor data input bit 2. (internal pull low)	
95	RGB3	I	Sensor data input bit 3. (internal pull low)	
96	RGB4	I	Sensor data input bit 4. (internal pull low)	
97	RGB5	I	Sensor data input bit 5. (internal pull low)	
98	RGB6	I	Sensor data input bit 6. (internal pull low)	
99	RGB7	I	Sensor data input bit 7. (internal pull low)	
100	RGB8	I	Sensor data input bit 8. (internal pull low)	

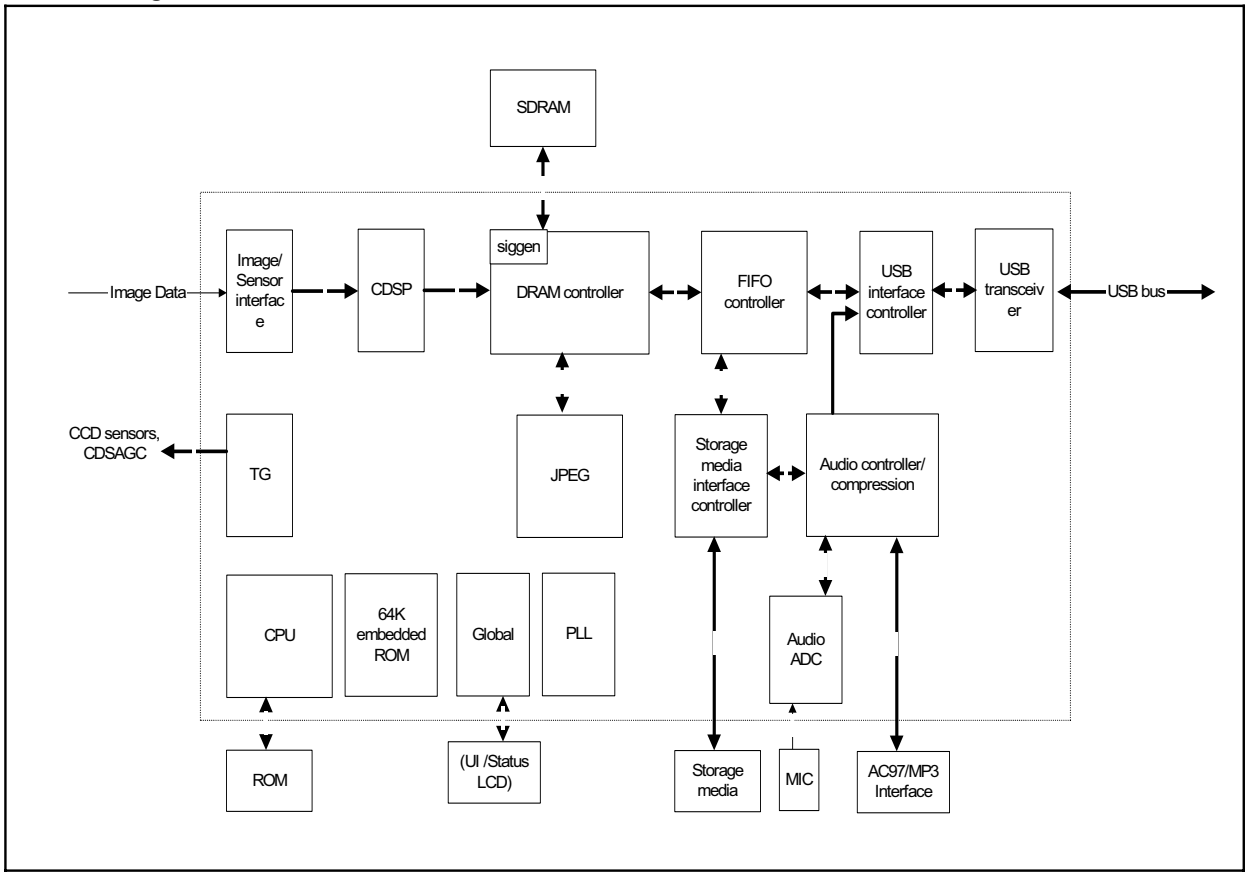
Pin No.	Pin Name	Direction	Description			Memo
101	RGB9	I	Sensor data input bit 9. (internal pull low)			
Timing Generator						
			Default function	TG disabled		
102	V1	B	Clock output for vertical CCD drive	EXTvd (B)		Note 6
103	V2	B	Clock output for vertical CCD drive	EXThd (B)		Note 6
104	V3	B	Clock output for vertical CCD drive	EXTvvalid (I)	GPIO15	Note 6
105	SG	B	CCD readout pulse	EXThvalid (I)	GPIO16	Note 6
106	SUB	O	CCD electric charge sweep pulse output.	EXTdvalid (I)	GPIO17	Note 6
107	OVDD4	PG	Timing generator IO PAD power			3.3V
108	OVSS4	PG	Timing generator IO PAD ground			
109	ADCLP	B	Dummy pixel clamping signal	2XCK output		Note 6
110	ADCK	B	Clock output for AD converter.	1XCK output		Note 6
111	SEN	O	Serial interface data transaction starting signal The SPCA504B has a built-in synchronous serial interface to communicate with the CDS/AGC chip. The CDS/AGC chip is needed when the SPCA504B is connected with a CCD image sensor.		GPIO26	
112	SCK	O	CDS/AGC serial interface clock.	SSISCL		Note 6
113	SD	B	CDS/AGC interface data output.	SSISDA		Note 6
114	DVDD4	PG	Core ground			2.5V
115	DVSS4	PG	Core power			
Built-in Audio ADC						
116	AVSSD	PG	ADC ground (digital)			
117	AVSS	PG	ADC ground (analog)			
118	ALC	I	AGC gain control			
119	MIC	I	Microphone analog input			
120	OPI	I	AGC OpAmp input			
121	OPO	O	AGC OpAmap output			
122	AVDD	PG	ADC power (analog)			3.3V
123	VREF	O	ADC voltage reference			
USB Transceiver						
124	UVSS	PG	USB transceiver ground			
125	DP	B	USB D+ signal			
126	DM	B	USB D- signal			
127	UVDD	PG	USB transceiver power			3.3V
128	SUSPEND	O	Chip suspend output		GPIO27	

Note* When the 128-pin package is selected, FMGPIO8 to FMGPIO19 are multiplexed to MD0 to MD11.

Note 1-6 Please refer to Note 1-6 in Section 3.1 for the function descriptions while ignoring the pin numbers.

4.FUNCTIONAL DESCRIPTION

4.1. Block Diagram



The figure shown above is a functional block diagram of the SPCA504B chip. The SPCA504B has two types of interface for image acquisition: CCD sensor and CMOS sensor. A timing generator (TG) module is designed to provide all the necessary clocking signals for the CCD sensor. The TG module must be disabled when the CMOS sensor is used. CMOS and CCD sensor data share the same digital input bus. A synchronous serial interface is used to program the CMOS sensor internal registers.

The external DRAM device serves as a buffer for capturing image frames as well as compressed data. Data access to the external DRAM memory is through a DRAM interface control module. Either the captured image or the image after CDSP processing can be stored in the external DRAM memory. CDSP is a color image processor that handles all color management and image enhancement functions. After the JPEG compression module, the compressed image can be buffered in the external DRAM before going to the USB interface or storage media interface. The JPEG compression engine can generate JFIF compliant bit streams.

The SPCA504B camera chip supports many types of storage media, such as, flash memory, smart media card, compact flash card, MultiMediaCard, SD card, and ATAPI interface. It also integrates a USB transceiver for transferring compressed image data to a PC.

This chip also includes a bi-directional audio control interface for MP3 audio and AC97 codec functions. When an AC97 codec is connected, the audio interface controller transfers audio data between the AC97 codec and the USB transceiver. The USB transceiver will further transfer the audio data between the SPCA504B chip and the host PC. Thus, the host PC can store the audio data recorded by the AC97 codec, and the AC97 codec and can then playback the audio data generated from the host PC.

The SPCA504B chip also includes an on-chip audio DAC for audio recording. It can connect to an external microphone directly. The audio compression is ADPCM. The compressed audio data

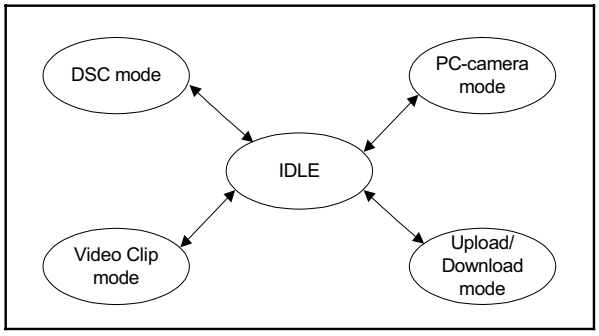
goes to the host PC through the USB interface.

The SPCA504B camera chip has integrated an 8032-compatible micro-controller with 4K bytes of on-chip SRAM data. The application programs can be stored in the 64K bytes of on-chip mask-ROM.

There are two on-chip PLL modules. The first is designed to generate an internal 48MHz master clock from an external 6, 12 or 24 MHz crystal. The other is used to generate clock signals for the CCD TG module.

4.2. Camera Operation Modes

The SPCA504B has five camera operation modes including *IDLE, DSC, PC-CAM, Video-Clip and Upload/download* modes. The mode transition is controlled by the firmware. Register 0X2000 defines the camera operation mode. The SPCA504B enters the designated mode immediately after the *Cam mode* register is programmed. All unfinished tasks are abandoned once the mode is changed.



IDLE mode - The IDLE mode is the default mode after the SPCA504B is power-on. The IDLE mode resets most of the internal modules to their power-on states except that the register values are preserved. Note that the CDSP module is in operation in the *IDLE* mode because it must provide the CPU with AE/AWB information.

DSC mode - Digital Still Camera mode is used to take a single still picture and saves the compressed image into the storage media. The embedded CPU is required to finish all the AE and AWB adjustments before the camera is put into the *DSC* mode. Once the camera enters the DSC mode, it captures the image and stores it in DRAM. The compression and storage tasks are controlled by the firmware. The firmware may instruct the SPCA504B to compress the image many times until the size of the compressed image meets the requirements.

Video-Clip mode - This mode is designed to take a sequence of pictures. The images can be temporarily saved in DRAM or directly passed to the storage media. The audio data can be taken (and compressed) at the same time and stored with the short video. Both video and audio compression are done by hardware. Moving data from the DRAM to the storage media is controlled by the firmware.

PC-Camera mode - While operating in this mode, the SPCA504B acts like a PC-camera. The image is taken, processed, compressed and passed to the PC via the USB bus continuously. The audio data can be sent to the PC at the same time via another USB pipe. USB ISO pipes are used in this mode. The firmware does nothing except AE/AWB adjustments in this mode.

Upload/Download mode - This mode is for data transfer from the PC to the camera and vice versa. For example, the images stored in the storage media can be sent to the PC via the USB bus in this mode. Data from the PC can be loaded into the camera in this mode (For example the updated firmware code). Normally, the BULK-IN or BULK-OUT pipes of the USB are used in this mode.

5.ELECTRICAL SPECIFICATIONS

5.1. Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Voltage on any pin relative to VSS	V_T	-0.4 to 4.0	V
Supply Voltage relative to VSS	V_{DD}	-0.4 to 4.0	V
Short Circuit Output Current	I_{OUT}		mA
Power Dissipation	P_D	0.3	W
Operating Temperature	T_{OPT}	0 to +70	°C
Storage Temperature	T_{STG}	-55 to 125	°C

5.2. DC Characteristics

I/O Pads: Vdd - Vss = 3.3V，T_A = 25 ℃

Characteristics	Symbol	Limit			Unit
		Min	Typ	Max	
I/O Operating Voltage	V_{DD}	3.0	3.3	3.6	V
Power supply current (unconfigured)	I_{DD}	-	10.0	-	mA
Power supply current (normal)	I_{DD}	-	18.0	-	mA
Power supply current (suspend)	I_{DD}	-	-	5.0	µA
Input High Level	V_{IH}	0.7VDD	-	VDD+10%	V
Input Low Level	V_{IL}	-0.3	-	0.3VDD	V
Output High I	I_{OH}	-	-4	-	mA
Output Sink I	I_{OL}	-	4	-	mA
Schmitt trigger positive-going threshold	V_{T+}	1.9	2.0	-	V
Schmitt trigger negative-going threshold	V_{T-}	-	1.1	1.2	V
Input leakage current	I_{IL}	-	-	1	µA

Core Logic: Vdd-Vss =2.5V，T_A = 25 ℃

Characteristics	Symbol	Limit			Unit
		Min	Typ	Max	
Core Operating Voltage	V_{DD}	2.25	2.5	2.75	V
Power supply current (unconfigured)	I_{DD}	-	36	-	mA
Power supply current (normal)	I_{DD}	-	56	-	mA
Power supply current (suspend)	I_{DD}	-		30	µA

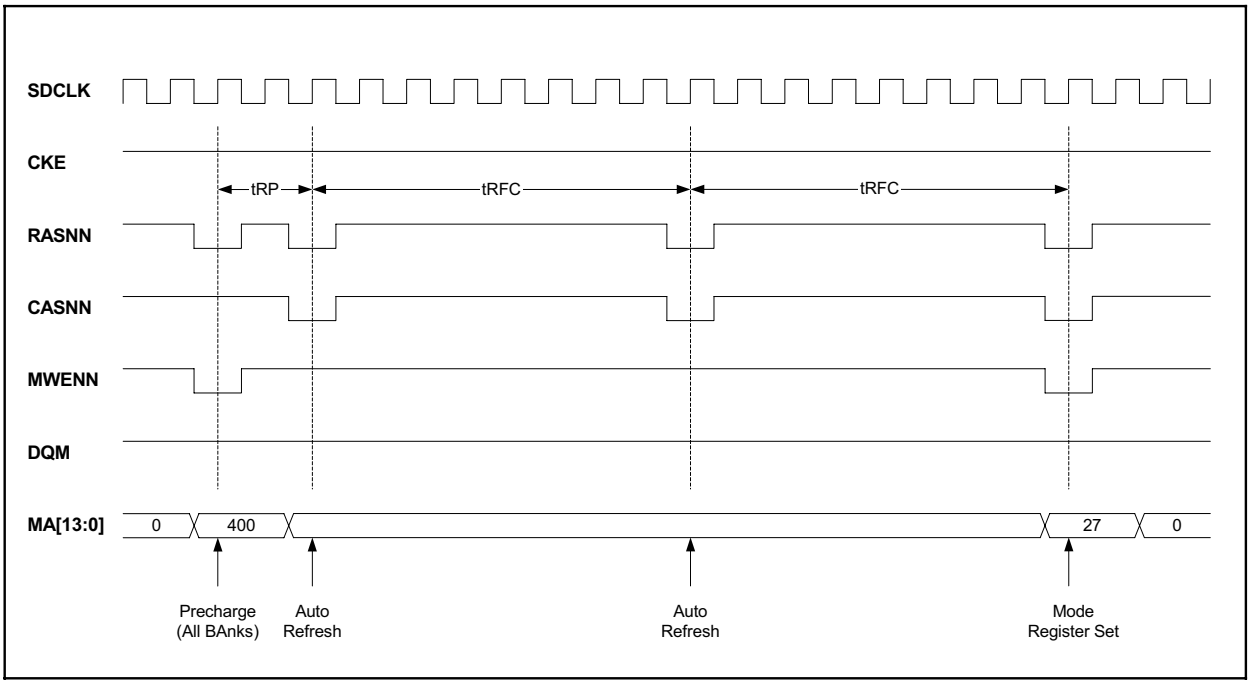
5.3. USB DC Characteristics

(for pin: DP, DM)

Symbol	Parameter	Min.	Max.	unit
V_{OCRS}	Output Signal Crossover voltage	1.3	2.0	V
V_{ICRS}	Input Signal Crossover voltage	0.8	2.5	V
V_{IL}	Input low voltage	-	0.8	V
V_{IH}	Input high voltage	2.0	-	V
V_{DI}	Differential Input Sensitivity	0.2	-	V

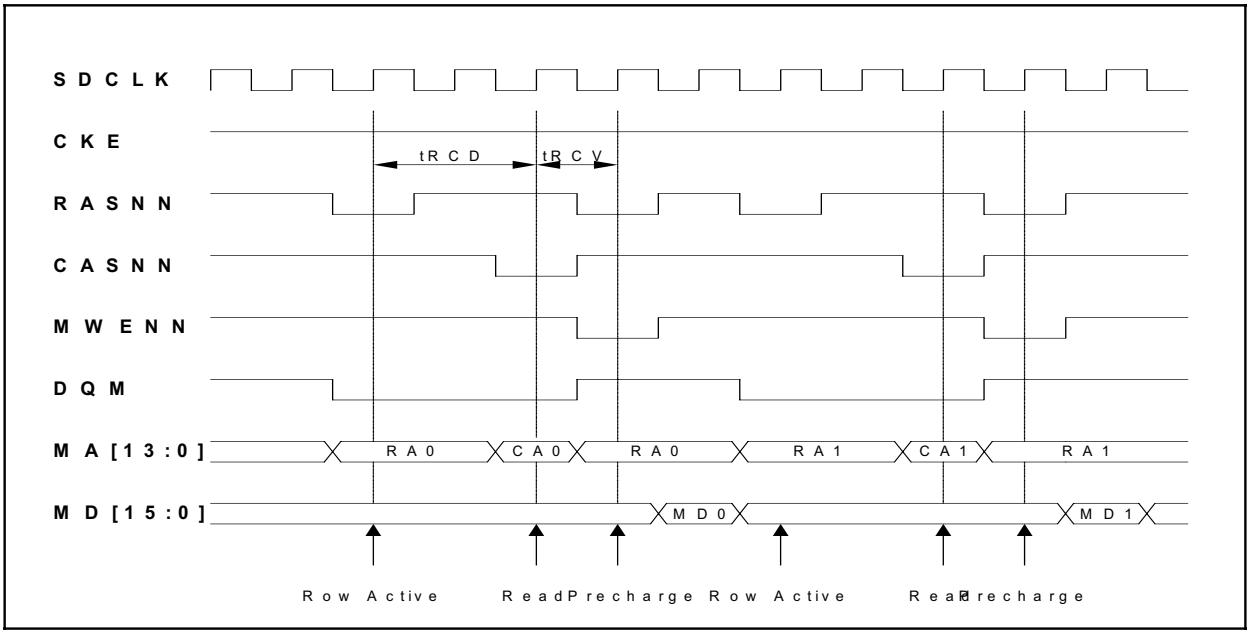
5.4. SDRAM Timing Characteristics

5.4.1. SDRAM initialization timing



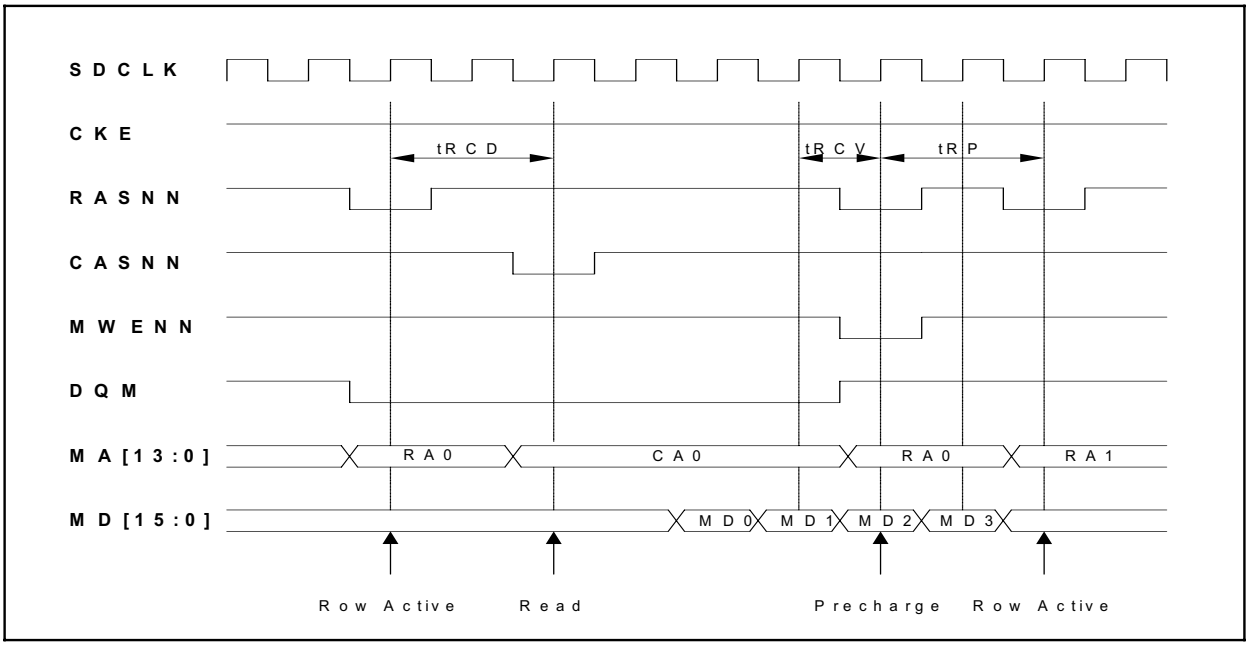
Time	Description	Min	Typ	Max	Units
tRP	Row precharge time	40	-	-	ns
tRFC	Auto refresh cycle time	160	-	-	ns

5.4.2. SDRAM single read timing



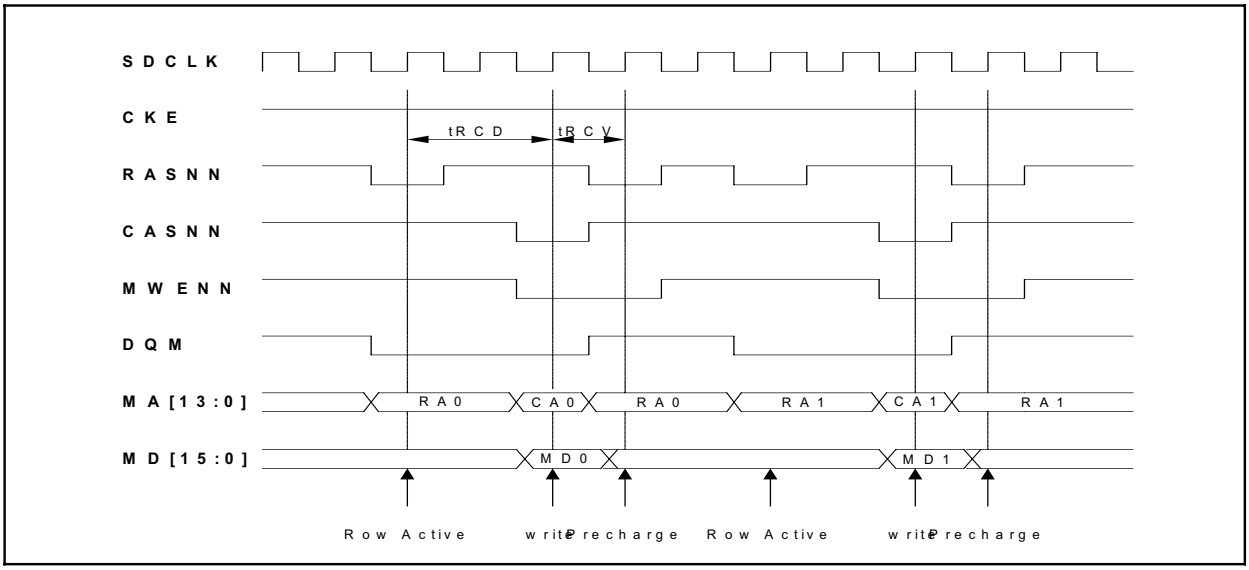
Time	Description	Min	Typ	Max	Units
tRCD	RAS to CAS delay	40	-	-	ns
tRCV	Recovery time	20	-	-	ns

5.4.3. SDRAM page mode read timing



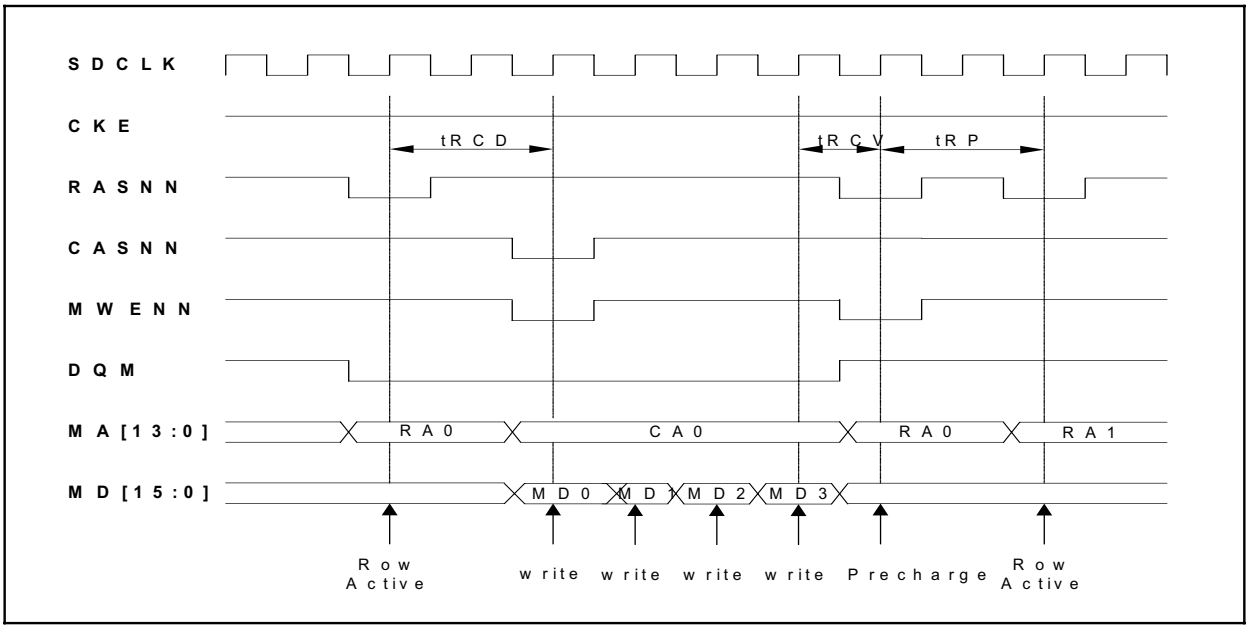
Time	Description	Min	Typ	Max	Units
tRCD	RAS to CAS delay	40	-	-	ns
tRCV	Recovery time	20	-	-	ns
tRP	Row precharge time	40	-	-	ns

5.4.4. SDRAM single write timing



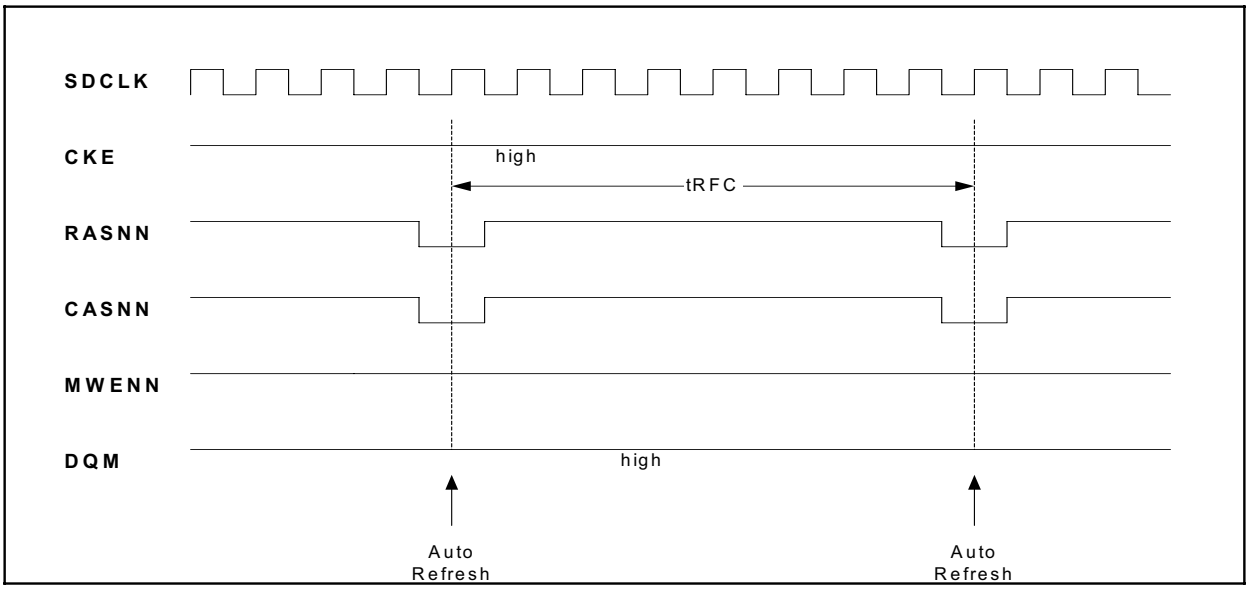
Time	Description	Min	Typ	Max	Units
tRCD	RAS to CAS delay	40	-	-	ns
tRCV	Recovery time	20	-	-	ns

5.4.5. SDRAM page mode read timing



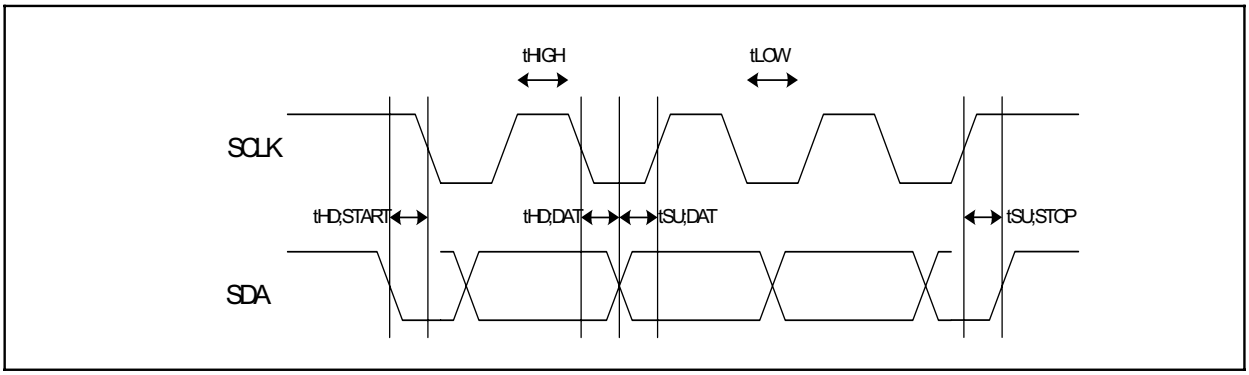
Time	Description	Min	Typ	Max	Units
tRCD	RAS to CAS delay	40	-	-	ns
tRCV	Recovery time	20	-	-	ns
tRP	Row precharge time	40	-	-	ns

5.4.6. SDRAM auto refresh timing



Time	Description	Min	Typ	Max	Units
tRFC	Auto refresh cycle time	160	-	-	ns

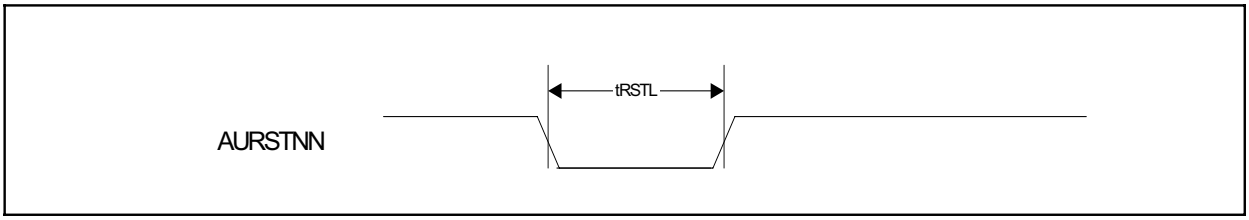
5.5. Synchronous Serial Interface Timing



Time	Description	Min	Typ	Max	Units
tHIGH	High period of SCLK	5.2	-	-	µs
tLOW	Low period of SCLK	5.2	-	-	µs
tHD;DAT	Data hold time	2.5	-	-	µs
tSU;DAT	Data set-up time	2.5	-	-	µs
tHD;START	Hold time for start condition	2.5	-	-	µs
tSU;STOP	Set-up time for stop condition	2.5	-	-	µs

5.6. AC-97 Interface Timing

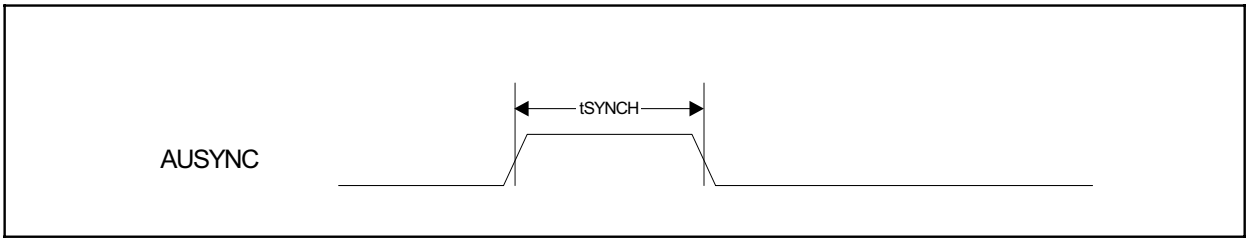
5.6.1. Cold Reset



Time	Description	Min	Typ	Max	Units
tRSTL	Active low pulse width	-	10	-	µs

* Programmable

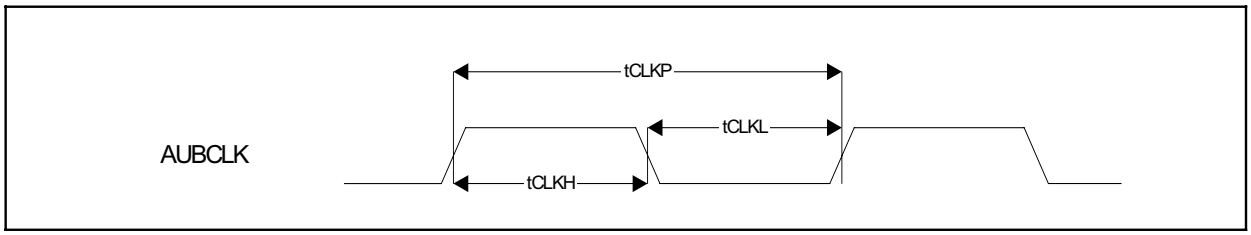
5.6.2. Warm Reset



Time	Description	Min	Typ	Max	Units
tSYNCH	Active high pulse width	-	1.3	-	µs

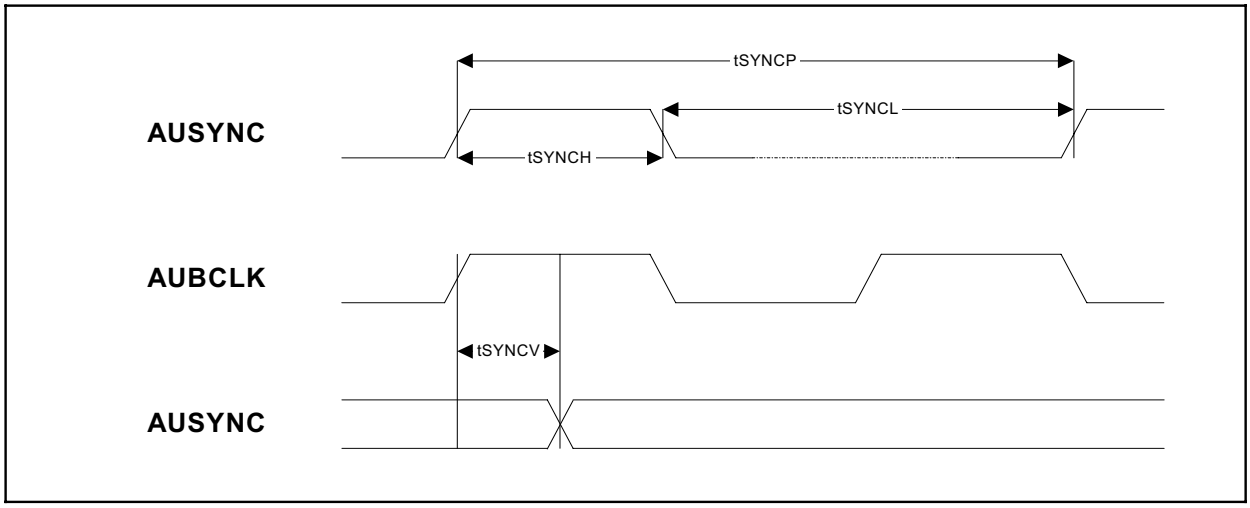
* Programmable

5.6.3. Clock Timing



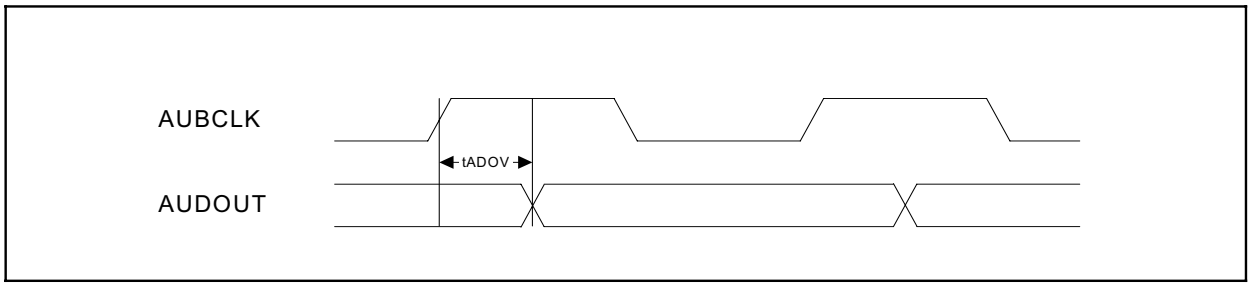
Time	Description	Min	Typ	Max	Units
tCLKH	Clock high pulse width	-	40.7	-	ns
tCLKL	Clock low pulse width	-	40.7	-	ns
tCLKP	Clock cycle time	-	-	-	ns

5.6.4. Sync Timing



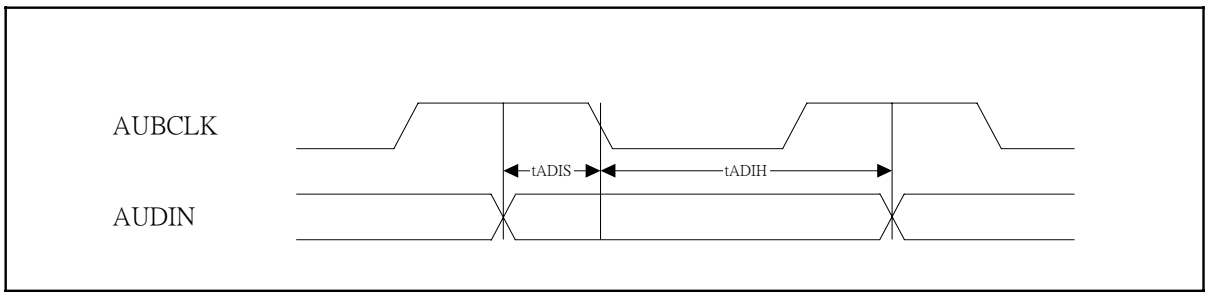
Time	Description	Min	Typ	Max	Units
tSYNCH	SYNC high pulse width	-	16	-	aubclk
tSYNCL	SYNC low pulse width	-	240	-	aubclk
tSYNCP	SYNC period	-	256	-	aubclk
tSYNCV	SYNC valid delay	-	-	25	ns

5.6.5. Audio data output timing



Time	Description	Min	Typ	Max	Units
tADOV	AUDOUT valid delay	-	-	15	ns

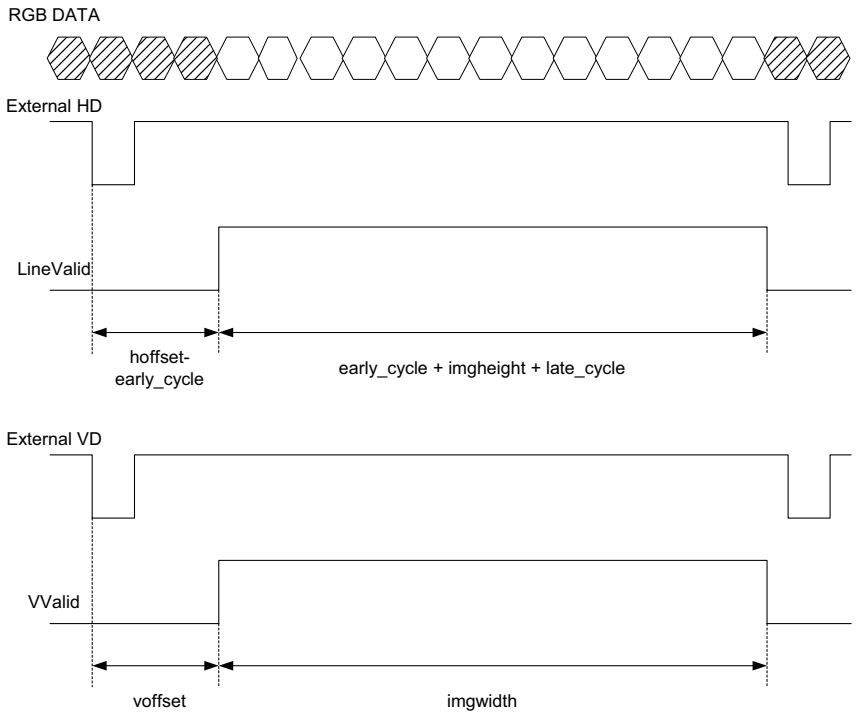
5.6.6. Audio Data Input Timing



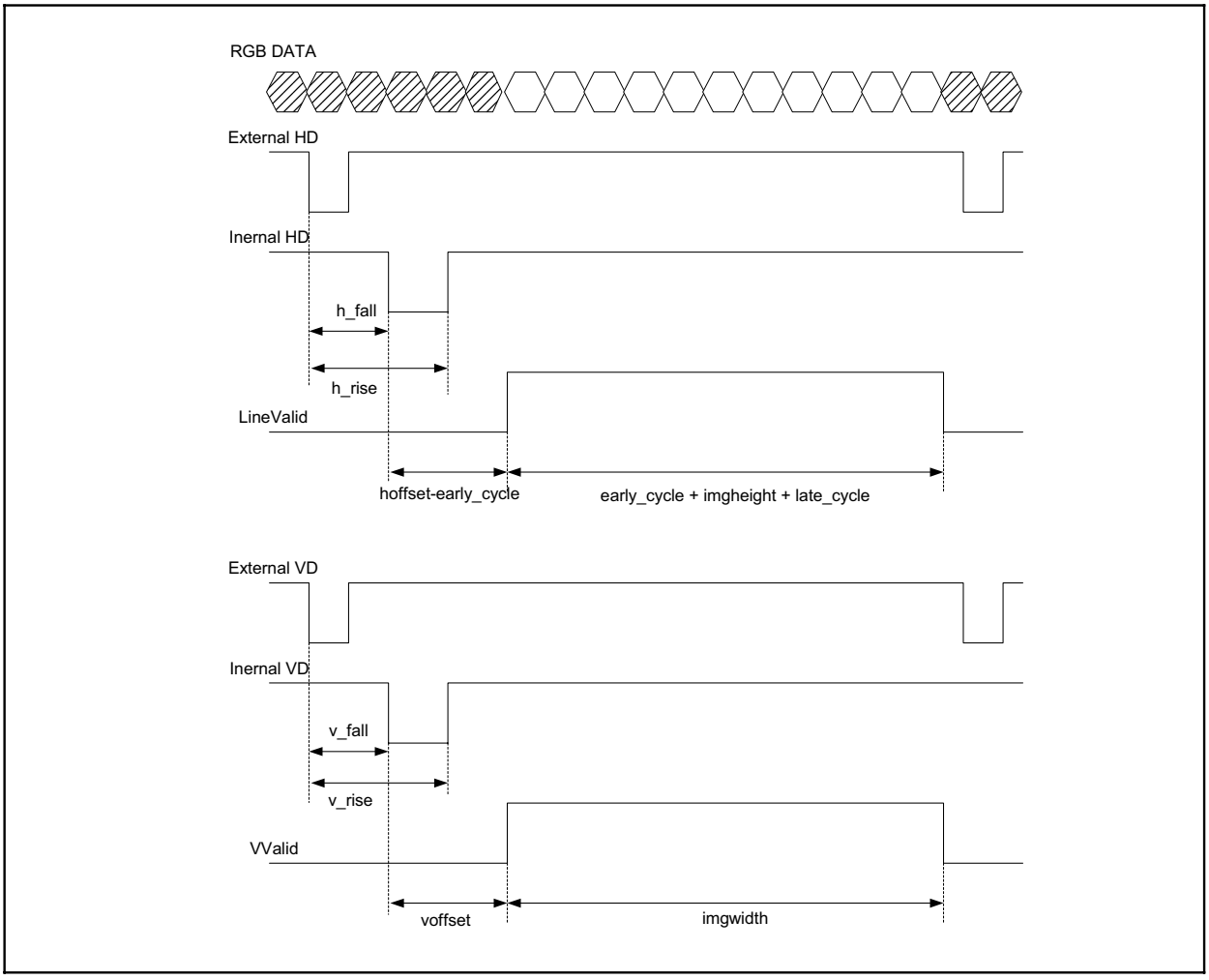
Time	Description	Min	Typ	Max	Units
tADIS	AUDIN setup time	10	-	-	ns
tADIH	AUDIN hold time	5	-	-	ns

5.7. CMOS Image Sensor Timing

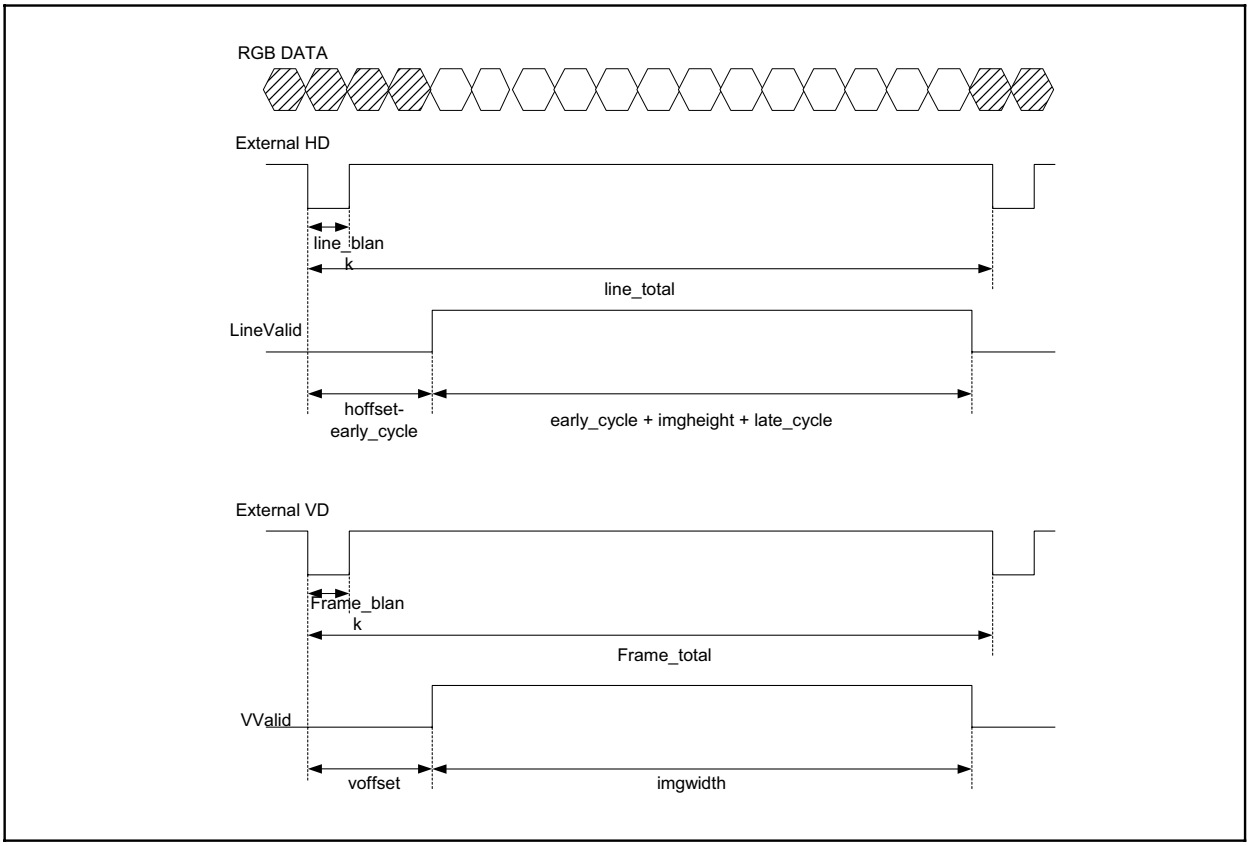
5.7.1. Original CMOS timing



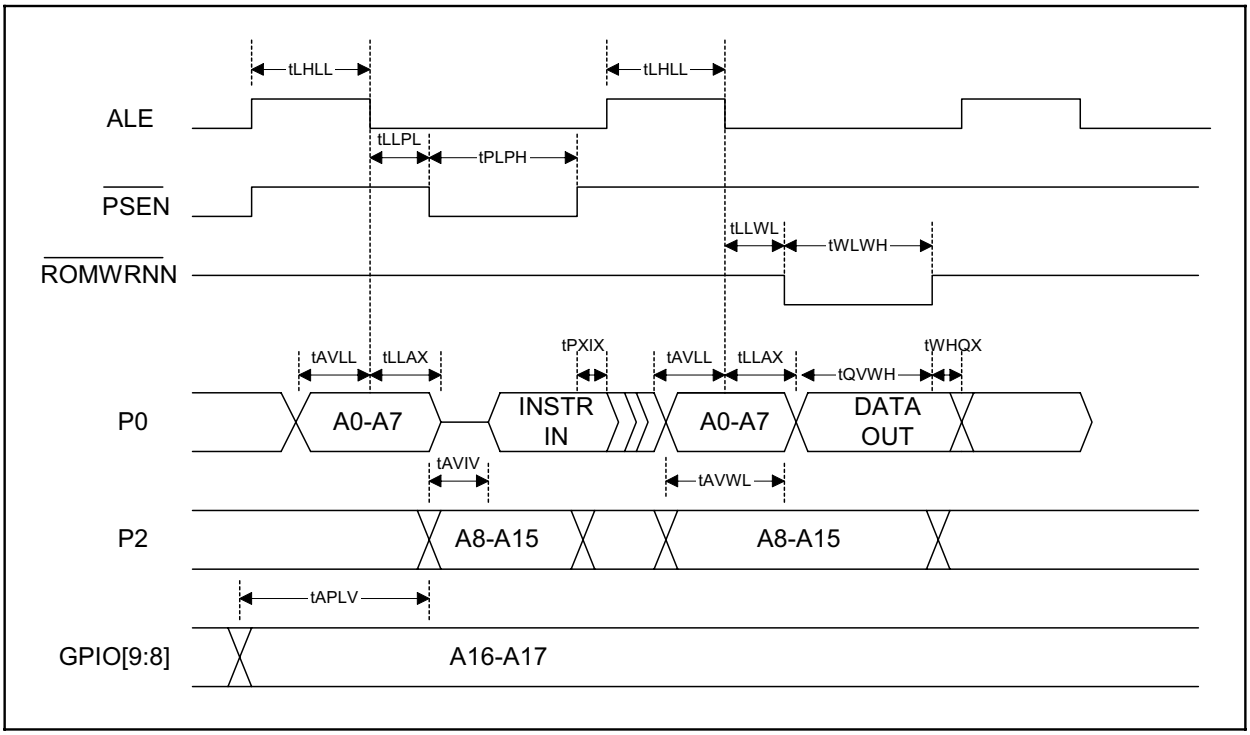
5.7.2. CMOS Image Sensor Reshapnig Timing



5.7.3. CMOS Image sensor programmable valid timing



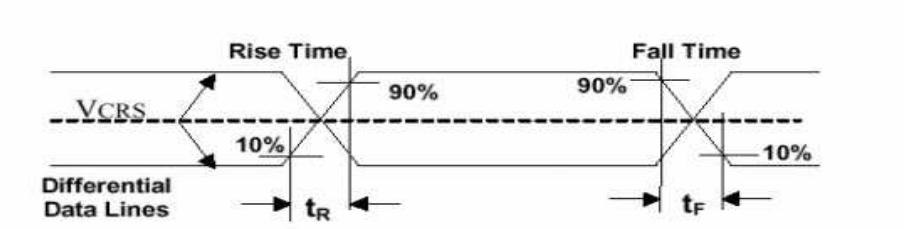
5.8. CPU Timing



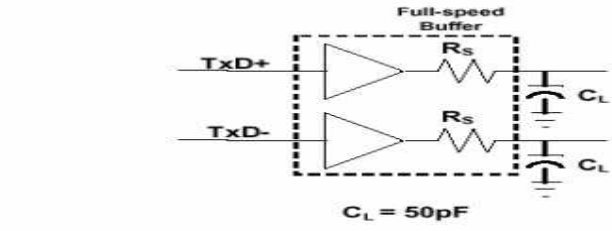
Time	Description	Min	Typ	Max	Units
tLHLL	ALE pulse width	50	-	-	ns
tLLPL	ALE low to PSEN low	20	-	-	ns
tPLPH	PSEN pulse width	80	-	-	ns
tLLWL	ALE low to ROMWRNN low	20	-	-	ns
tWLWH	ROMWRNN pulse width	80	-	-	ns
tAVLL	Address valid to ALE low	14	-	-	ns
tLLAX	Address hold after ALE low	20	-	-	ns
tPXIX	Input instrustion hold after PSEN	0	-	-	ns
tQVWH	Data valid to ROMWRNN high	75	-	-	ns
tWHQX	Data hold after ROMWRNN	40	-	-	ns
tAVIV	Address to valid in	-	-	70	ns
tAVWL	Address to ROMWRNN low	38	-	-	ns
tAPLV	Address to PSEN low	80	-	-	ns

5.9. USB Timing

Driver Characteristics:



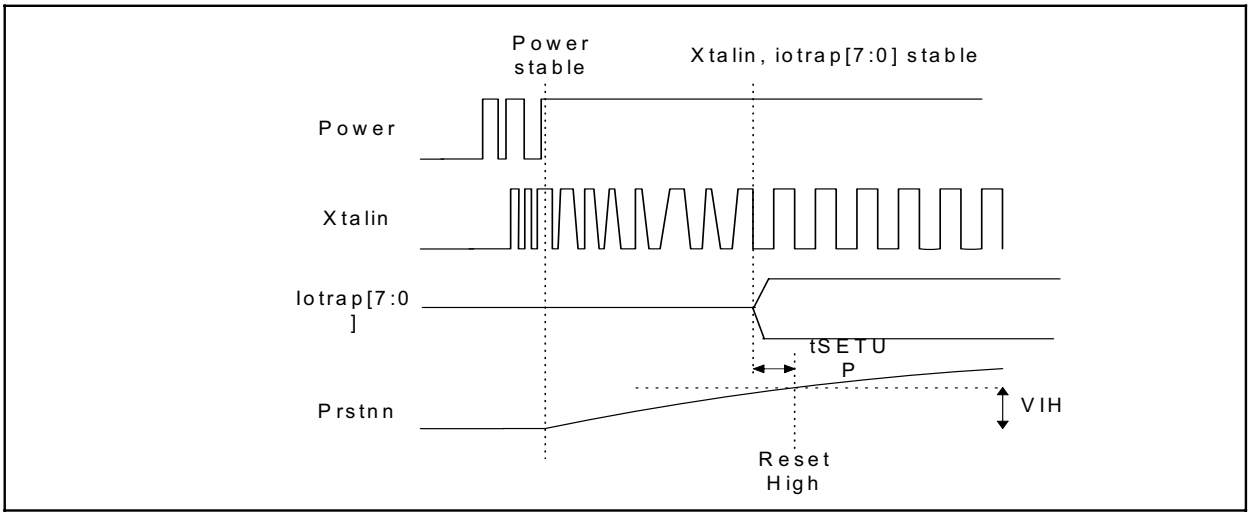
Parameter	Symbol	Condition	Min	Max	Unit
Rise Time	tR	D+ and D- connect Rs (12 Ω) in serial，and 50pF to ground	4	20	ns
Fall Time	tF		4	20	ns
Differential Rise and Fall Time Matching	tRFM	(tR÷ tF)	90	111.11	%



Clock Timings:

Parameter	Symbol	Min	Max	Unit
Full-speed Data Rate	TFDRATE	11.9700	12.0300	Mb/s
Frame Interval	TFRAME	0.9995	1.0005	ms

5.10. Power-On Reset Timing

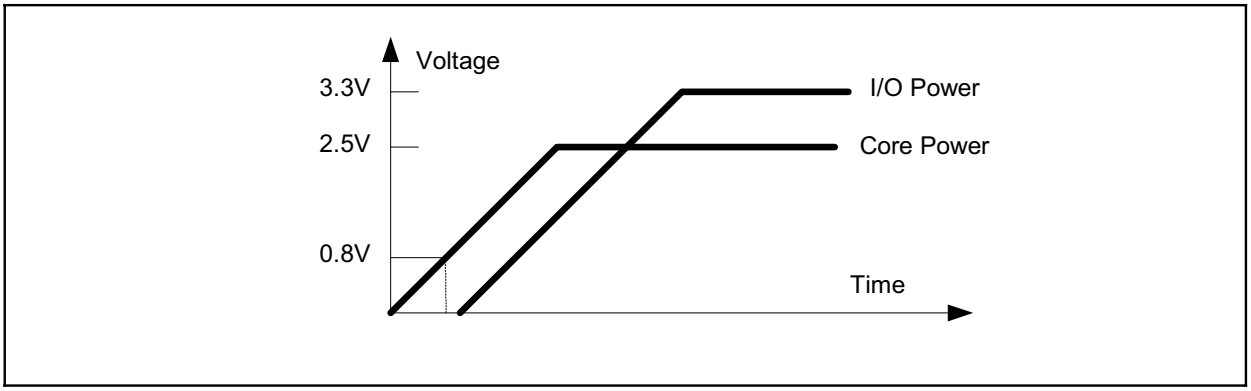


R1＝10K、C1＝2.2uF

Symbol	Parameter	Limit			Unit
		Min.	Typ.	Max.	
tSETUP	I/O Trap setup time	6	-	-	ms

5.10.1. Power-on Sequence

The following diagram shows the external power supply sequence for the SPCA504B. The power for the SPCA504B I/O pad will have a 0.8V voltage drop below core power if I/O power is not supplied. Note that there will be glitches on the I/O pads if I/O power is supplied before core power. If there are still small glitches on the I/O pads when the correct power-on sequence is applied, then adding suitable pull-down resistance on the corresponding I/O pads will suppress the glitches. There will be no glitches over 0.8V on I/O pads if the power-on sequence is followed and suitable pull-down resistors are added.



The power-on sequence diagram

Hence, the 2.5V core power must be supplied before the 3.3V I/O power is supplied. The power-on sequence is as follow.

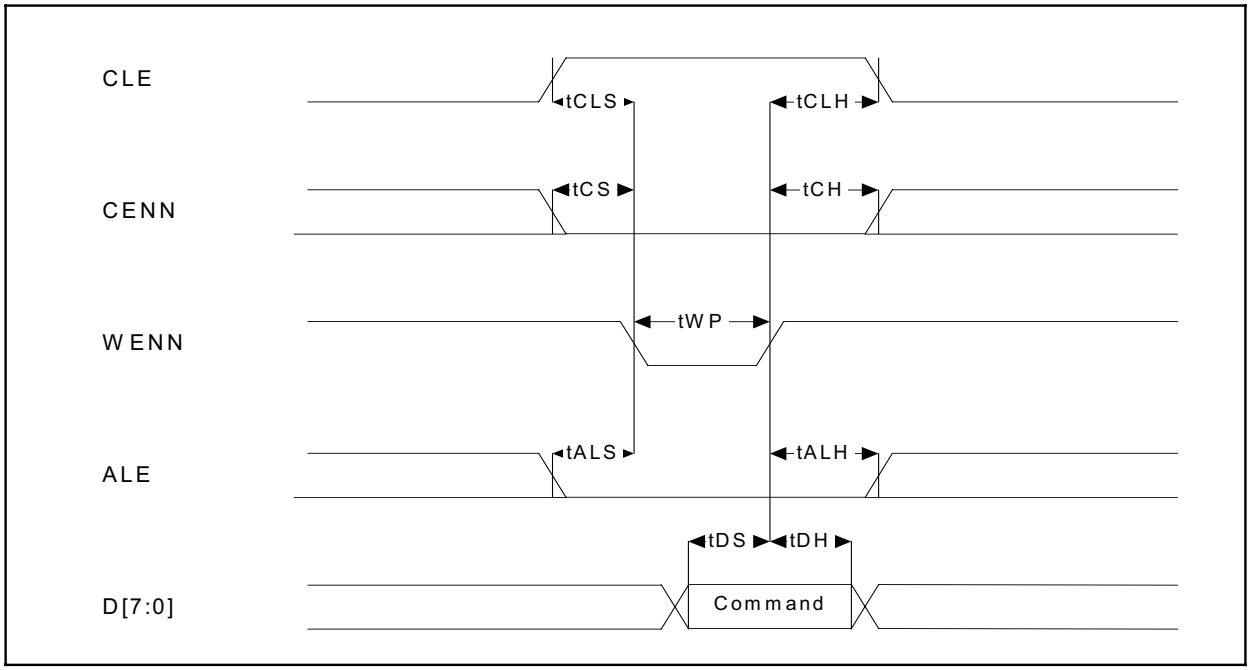
1.) Turn on the 2.5V core power.

2.) Turn on the 3.3V I/O power after the 2.5V core power reaches 0.8V.

3.) If necessary, I/O pads shall be pull-low with a 10K resistor to prevent any glitches.

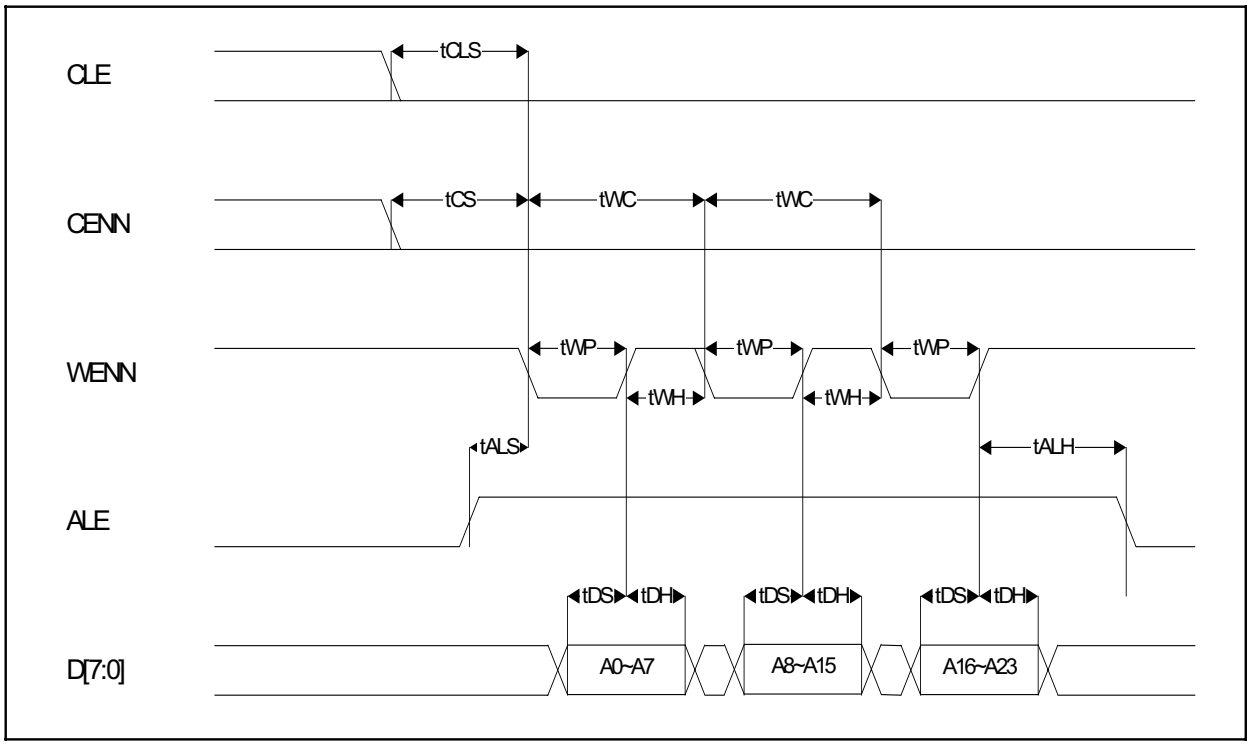
5.11. Flash Memory Interface Timing

5.11.1. Command Latch Cycle



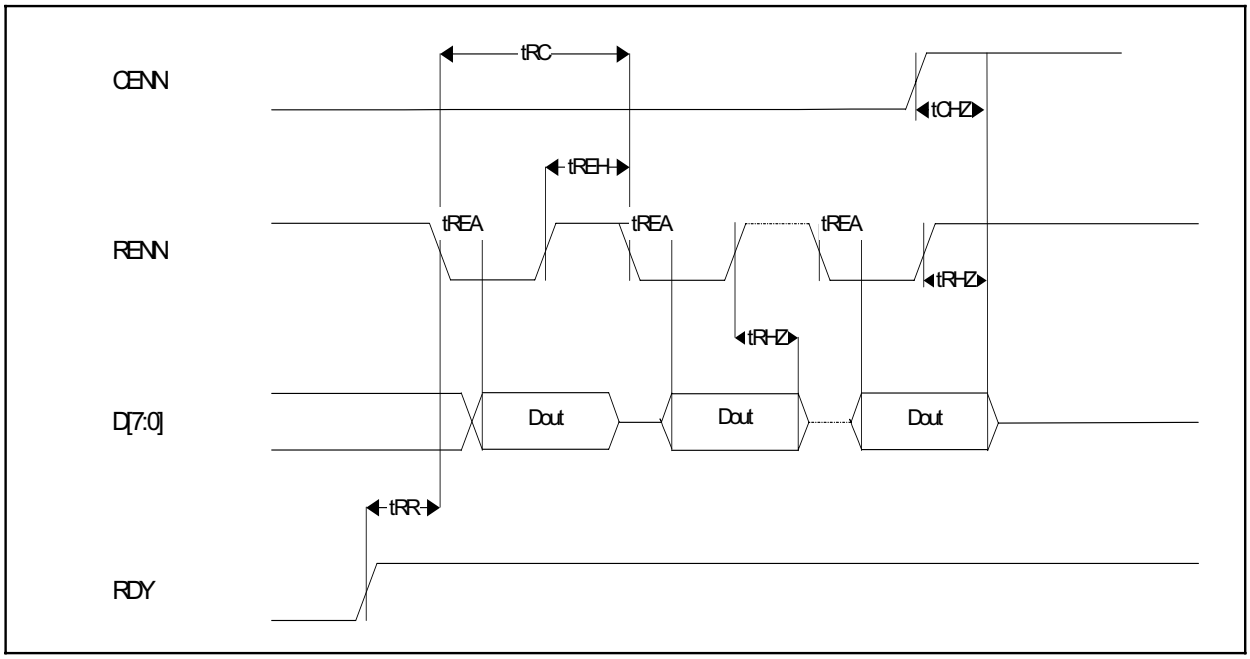
Time	Description	Min	Typ	Max	Units
tCLS	CLE setup time	1120	-	-	ns
tCLH	CLE hold time	1120	-	-	ns
tCS	CENN setup time	1120	-	-	ns
tCH	CENN hold time	1120	-	-	ns
tWP	WENN pulse width	80	-	-	ns
tALS	ALE setup time	1120	-	-	ns
tALH	ALE hold time	1120	-	-	ns
tDS	D[7:0] setup time	80	-	-	ns
tDH	D[7:0] hold time	20	-	-	ns

5.11.2. Address Latch Cycle



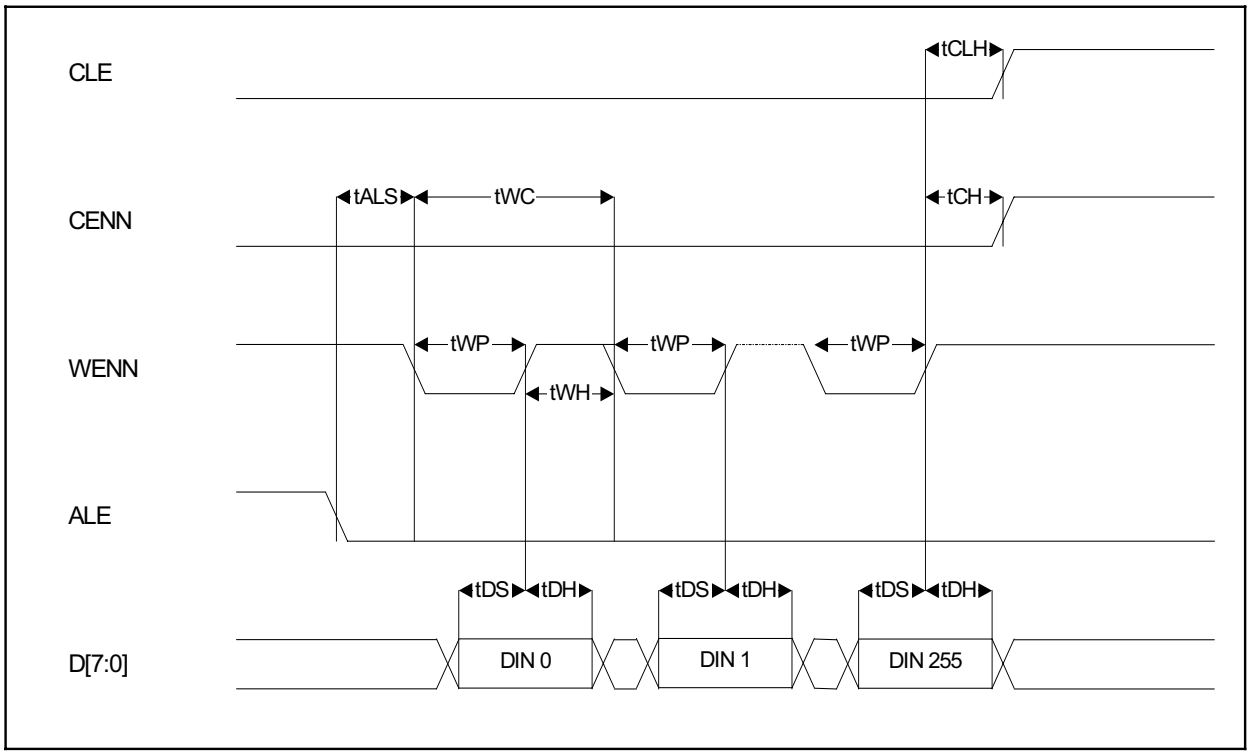
Time	Description	Min	Typ	Max	Units
tCLS	CLE setup time	1120	-	-	ns
tCS	CENN setup time	1120	-	-	ns
tWC	Write cycle time	320	-	-	ns
tWP	WENN pulse width	80	-	-	ns
tWH	WENN high hold time	240	-	-	ns
tALS	ALE setup time	1120	-	-	ns
tALH	ALE hold time	1120	-	-	ns
tDS	D[7:0] setup time	80	-	-	ns
tDH	D[7:0] hold time	20	-	-	ns

5.11.3. Sequential Out Cycle after Read



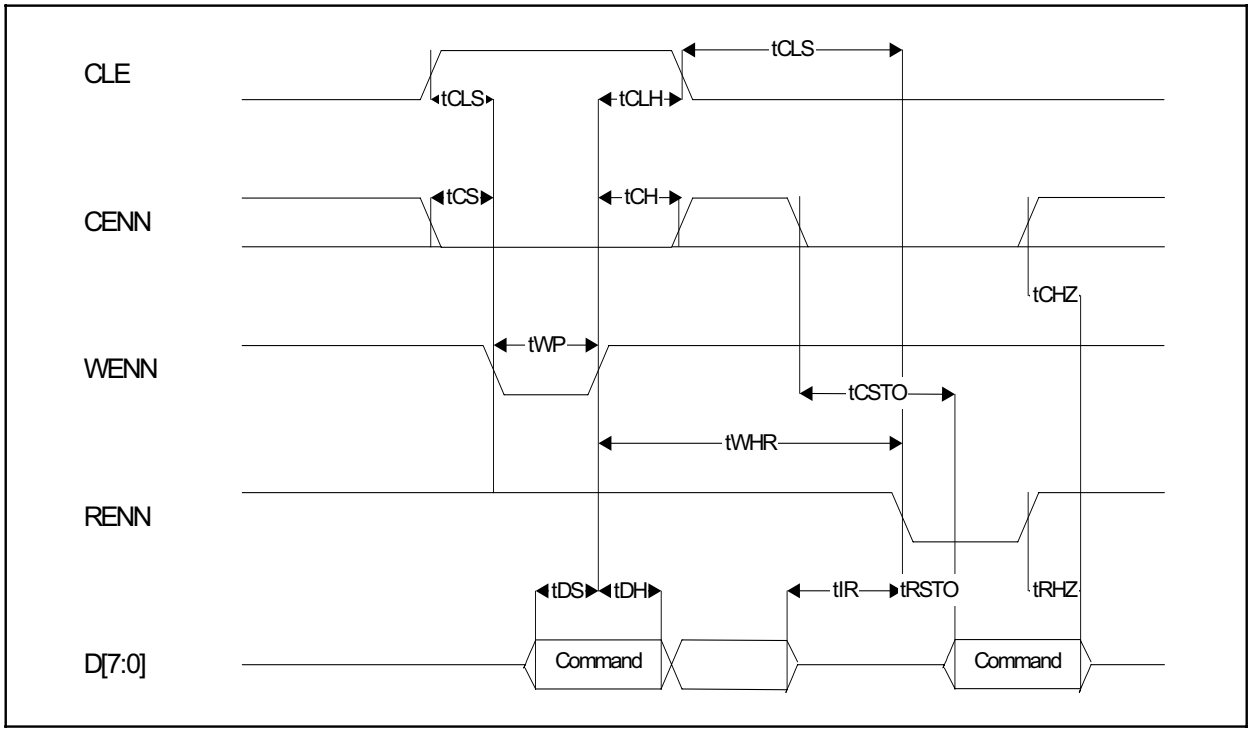
Time	Description	Min	Typ	Max	Units
tRC	Read cycle time	100	-	-	ns
tCHZ	CENN high to output Hi-Z	0	-	-	ns
tREA	RENN access time	-	-	50	ns
tREH	RENN high hold time	60	-	-	ns
tRHZ	RENN to D[7:0] output Hi-Z	0	-	-	ns
tRR	RDY to RENN low	1120	-	-	ns

5.11.4. Input Data Latch Cycle



Time	Description	Min	Typ	Max	Units
tCLH	CLE hold time	1120	-	-	ns
tALS	ALE setup time	1120	-	-	ns
tWC	Write cycle time	100	-	-	ns
tCH	CENN hold time	1120	-	-	ns
tWP	WENN pulse width	40	-	-	ns
tWH	WENN high hold time	60	-	-	ns
tDS	D[7:0] setup time	40	-	-	ns
tDH	D[7:0] hold time	40	-	-	ns

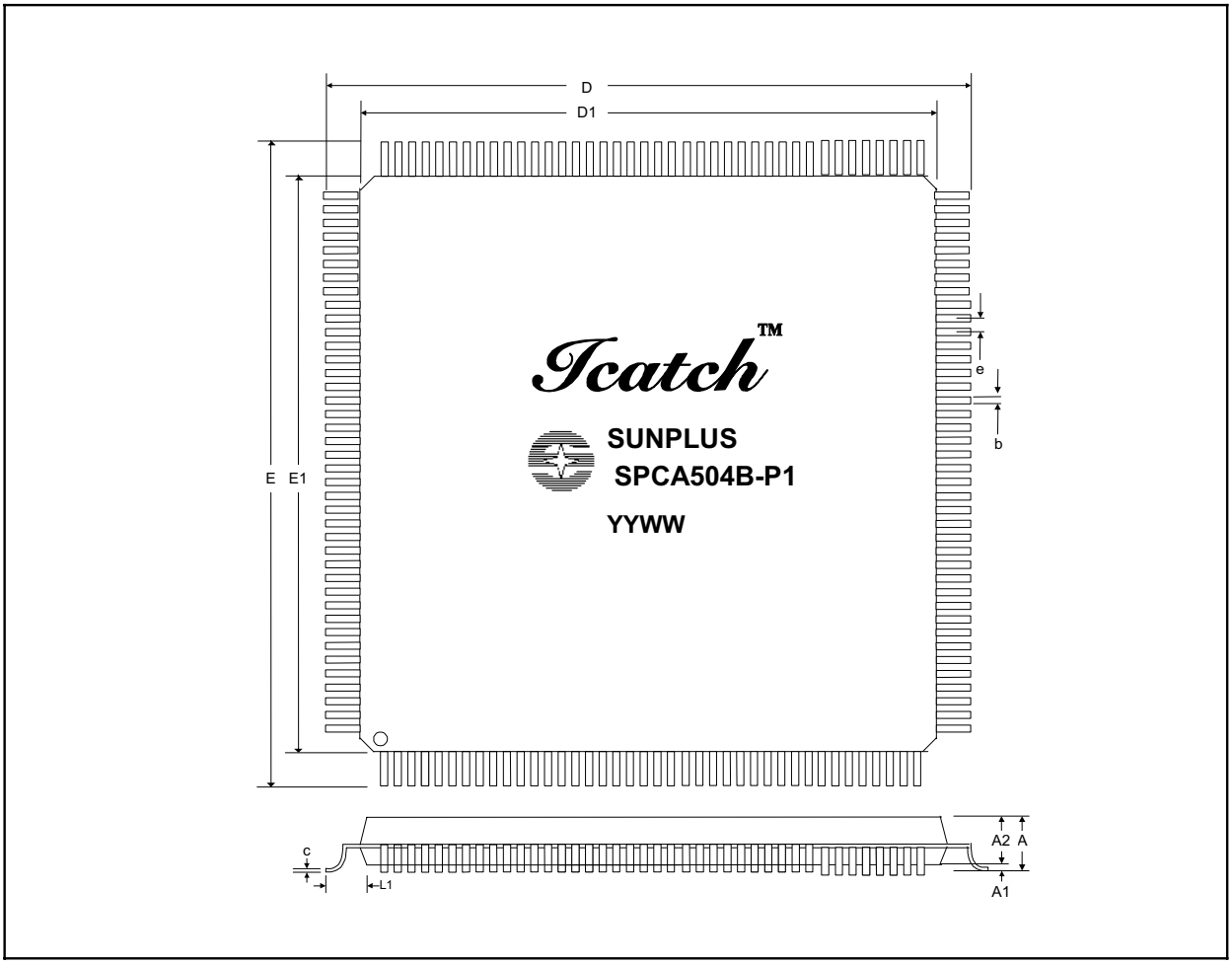
5.11.5. Status Read Cycle



Time	Description	Min	Typ	Max	Units
tCLS	CLE setup time	1120	-	-	ns
tCLH	CLE hold time	1120	-	-	ns
tCS	CENN setup time	1120	-	-	ns
tCH	CENN hold time	1120	-	-	ns
tWP	WENN pulse width	80	-	-	ns
tCHZ	CENN high to output Hi-Z	0	-	-	ns
tCSTO	CENN low to status output	-	-	1170	ns
tWHR	WENN high to RENN low	2240	-	-	ns
tDS	D[7:0] setup time	80	-	-	ns
tDH	D[7:0] hold time	20	-	-	ns
tIR	D[7:0] output Hi-Z to RENN low	0	-	-	ns
tRSTO	RENN to status output	-	-	50	ns
tRHZ	RENN to D[7:0] output Hi-Z	0	-	-	ns

6. PACKAGE

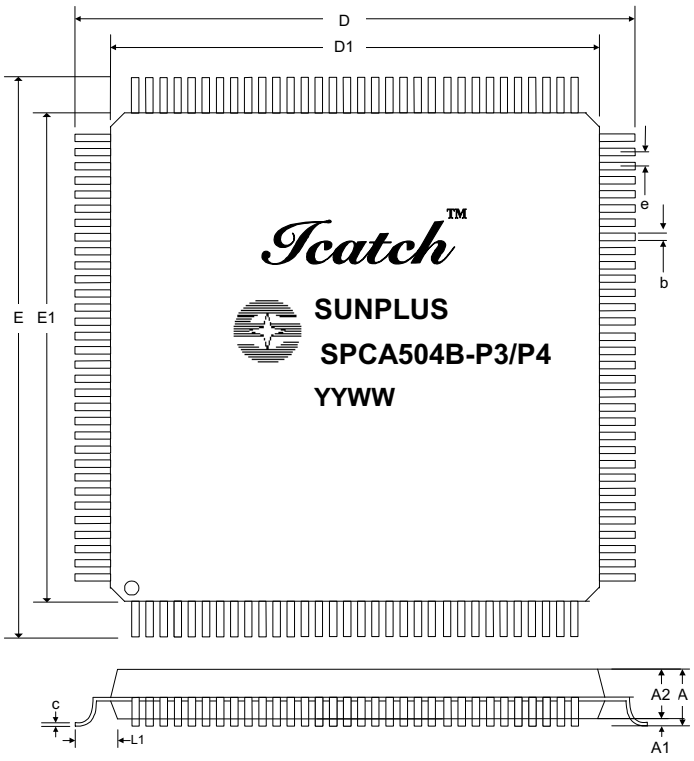
6.1. LQFP 160-pin



Symbol	Min.	Nom.	Max.
A	-	-	1.6
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D	-	22.00	-
D1	-	20.00	-
E	-	22.00	-
E1	-	20.00	-
L1	-	1.00	-
b	0.13	0.18	0.23
c	0.09	-	0.20
e	-	0.40	-

Unit: millimeter

6.2. LQFP 128-Pin



Symbol	Min.	Nom.	Max.
A	-	-	1.6
A1	0.05	-	-
A2	1.35	1.40	1.45
D	15.85	16.00	16.15
D1	13.90	14.00	14.10
E	15.85	16.00	16.15
E1	13.90	14.00	14.10
L1	-	1.00	-
b	0.13	0.18	0.23
c	0.09	-	0.20
e	-	0.40	-

Unit: millimeter

7.DISCLAIMER

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8.REVISION HISTORY

Date	Revision #	Description	Page
JUL. 16, 2003	0.1	Original	45